64000

HP 64000 Logic Development System

Model 64621A State Analysis Control Board

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its option, either repair or replace products which prove to be defective.

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For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

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ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

SERVICE MANUAL CHANGES

MANUAL IDENTIFICATION

Model Number: 64621A

Date Printed: June 1983

Part Number: 64621-90903

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement:

Make all ERRATA corrections.

Make all appropriate serial number related changes indicated in the tables below.

Serial Prefix or Number	Make Manual Changes	Serial Prefix or Number	Make Manual Changes
ALL			

▲ NEW ITEM

Model 64621A is now supported by the Bluestripe program, which means you should no longer perform component level troubleshooting on the board whose part number is listed here. The Bluestripe pipeline contains replacement boards for 64000 options made by Hewlett-Packard (replacement boards for this instrument are available at the factory). The part number for the replacement board is:

64621-69503

NOTE

Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. When requesting copies quote the manual identification information from your supplement, or the model number and print date from the title page of the manual.

Date: 7 March 1984
Page: 1 of 1

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READER COMMENT SHEET

Service Manual, Model 64621A
State Analysis Control Board
64621-90903, June 1983

Your comments are important to us. Please answer this questionaire and return it to us. Circle the number that best describes your answer in questions 1 through 7. Thank you.

1. The information in this book is complete:

Doesn't cover enough (what more do you need?)	1 2 3 4 5	Covers everything

2. The information in this book is accurate:

Too many errors	1 2 3 4 5	Exactly right

3. The information in this book is easy to find:

I can't find things I need	1 2 3 4 5	I can find info quickly

4. The Index and Table of Contents are useful:

Helpful	1 2 3 4 5	Missing or inadequate

5. What about the "how-to" procedures and examples:

No help	1 2 3 4 5	Very helpful
Too many now	1 2 3 4 5	I'd like more

6. What about the writing style:

Confusing	1 2 3 4 5	Clear

7. What about organization of the book:

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SERVICE MANUAL

MODEL 64621A
STATE ANALYSIS CONTROL BOARD

REPAIR NUMBERS

This manual applies to 64621A State Analysis Control Boards with a repair number prefix of 2311A. For further information on repair numbers refer to "Instruments Covered by This Manual" in Section I, and Section VII for Backdating to earlier Models.

LOGIC SYSTEMS DIVISION
COLORADO SPRINGS, COLORADO, U.S.A.

Manual Part No. 64621-90903

PRINTED: June 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

Table of Contents

Section V Adjustments

Section VI Replaceable parts

Section VII Manual Backdating

Section VIII Service

List of Figures and Tables

Figure or Table **Page**

Section I General Information

Section II Installation

Section III Operation

Section IV Performance Verification

Section V Adjustments

Section VI Replaceable Parts

Section VII Manual Backdating

Section VIII Service

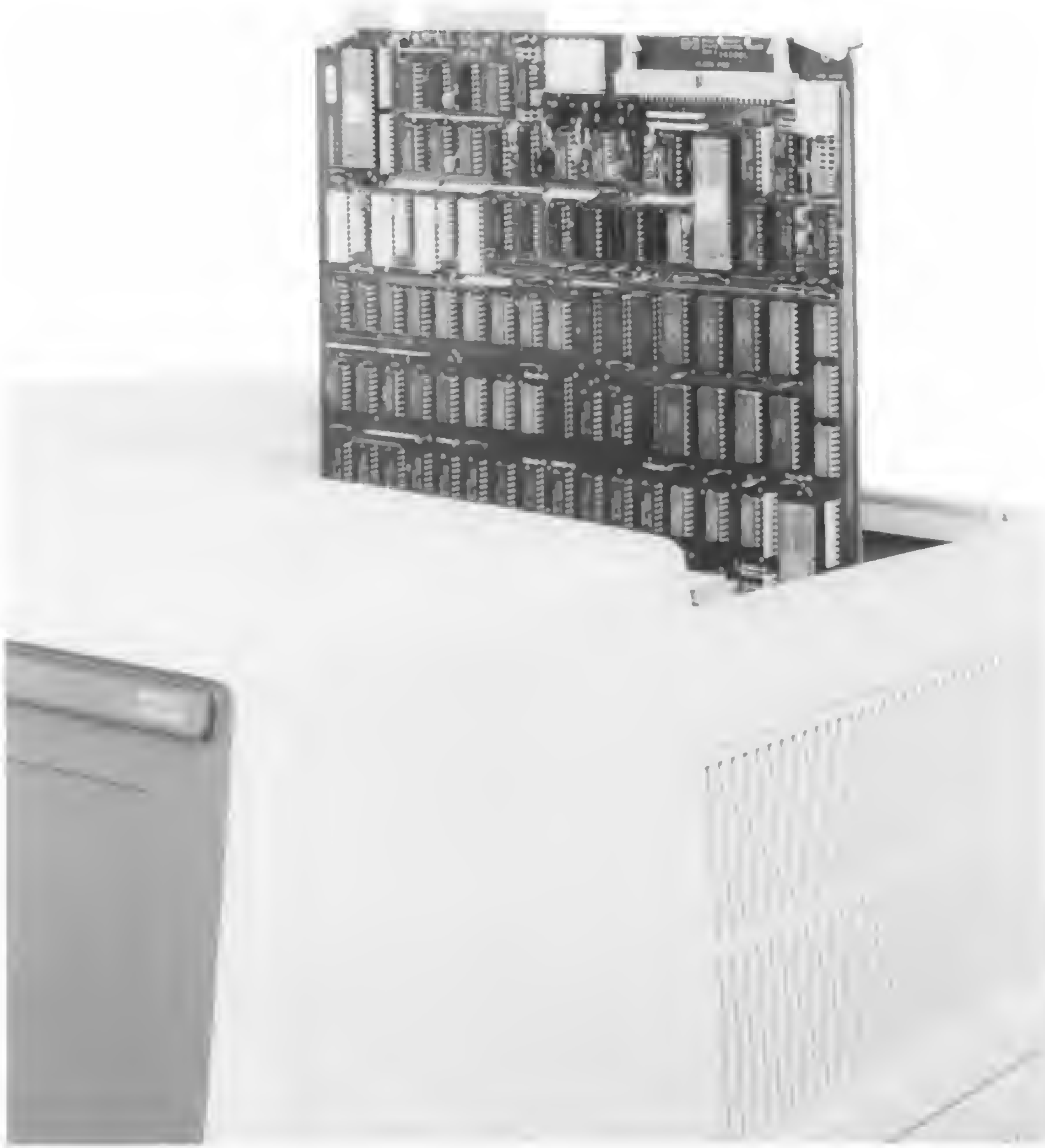


Figure 1-1. Model 64621A State Analysis Control Board

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64621A State Analysis Control Board (SAC). Operating instructions are provided in a separate Operating Manual supplied with the instrument. It should be kept with the instrument for use by the operator.

1-3. Shown on the title page is a microfiche part number. This number can be used to order 4x6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. SPECIFICATIONS.

1-5. Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2. lists supplemental characteristics. Supplemental characteristics are not specifications but are typical characteristics included as additional information for the user.

Table 1-1. Specifications

Includes Models 64621A Control Board, 64622A 40 Channel Acquisition, and 64623A 20 Channel Acquisition Boards with General Purpose Probes.

Unqualified Clock Rate: 25 MHz max.

Qualified Clock Rate: 10 MHz max.

Time Count: Accuracy 0.1% or 40 ns, whichever is greater.

Pulse Widths, Setup and Hold Times: all polarities.
- Clock Pulse Width - 20 ns min.
- Clock Qualifier Setup Time - time qualifier must be present prior to active edge of clock - 20 ns max.
- Clock Qualifier Hold Time - time qualifier must remain present and stable after active edge of clock - 0 ns.
- Data Setup Time - time data must be present prior to active edge of clock - 30 ns max.
- Data Hold Time - time data must remain present and stable after active edge of clock - 0 ns.

BNC Port Outputs (Mainframe Rearpanel): programmable polarity.
- Stimulus (Port 1) - TTL pulse output into 50 Ohms.
  - Occurs at each recognized event.
    - Trigger Events,
      - Pulse Width 50 ns +/- 20 ns.
      - Delay from clock 225 ns +/- 25 ns.
    - Sequencer Events,
      - Pulse Width 50 ns +/- 20 ns.

Table 1-1. Specifications (Cont'd)

Delay from clock 200 ns +/- 25 ns.
Halt (Port 2) - TTL level output into 50 Ohms.
False at execute, true at event recognition or halt.
Measurement Complete,
Delay from clock 225 ns +/- 25 ns.
Trace Point,
Delay from clock 225 ns +/- 25 ns.

Table 1-2. Supplemental Characteristics

Memory Size:
Width - expandable to 120 channels in combinations of 20 and/or 40 channel acquisition boards (max 3 ACQ boards).
Depth - Trace Storage - 256 locations.
Overview (Model 64623A only) - 4096 locations.

Sequence: Multiple function control with windows and qualifiers, occurrence, and restart.

Clocks: 8 ORed clocks and/or qualifiers.

Interactive Read of Trace Data: up to 4.75 MHz qualified clock rate.

Run Status:
Waiting for trigger.
Trace in process.
Overview in process.
Slow clock.
Measurement complete.

Overview Functions: (Model 64623A only).
Sequencer Windowed/Controlled.
3 Modes,
State Data.
Time Count, start to stop, 8.0 hrs max time within 40 ns or 0.1%.
Event Count, start to stop, count by one from 0 to 611,670; max count 750 X 10e+9.
3 Displays,
Overview Histogram.
Overview List.
Overview Graph.

IMB Functions (interconnection with other modules):
Master Enable (drive, receive).
Storage Enable (drive, receive).
Trigger Enable (drive, receive).
Trigger (drive, receive).
Delay Clock (drive only).

Table 1-2. Supplemental Characteristics (Cont'd)

20 Bit Ranging (Model 64623A only):
- Applicable to trace or overview functions.
- Four trace ranges or up to 15 overview ranges.
- Range on a contiguous subset of the 20 bits (right justified).

Trace Count Measurement:
- Windowing of time or state count.
- Stored State to Stored State,
  - Time Count - 8.0 hrs max time within 40 ns or 0.1%.
  - Event Count - count by one from 0 to 611,670, max count 750 X 10e+9.

Symbol Entry and Output:
- Definition of symbol maps in format specification.
- Use of symbols in Trace specification.
- Trace list uses symbols to present symbolic display.
- Each label may have its own or use another symbol map.

Probing Versatility:
- General Purpose Probes (Models 64635A and 64636A).
- General Purpose Preprocessor with dedicated interfaces.
  - See Model 64650A General Purpose Preprocessor Manual.

1-6. INSTRUMENTS COVERED BY THIS MANUAL.

1-7. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-8. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-9. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-10. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Office.

1-11. RECOMMENDED TEST EQUIPMENT.

1-12. Equipment required to maintain the Model 64621A is listed in Table 1-3. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-3. Recommended Test Equipment

4 1/2 Digit Multimeter accurate to +/-1 mV. (Hewlett-Packard Model 3466A or equivalent.)

Hewlett-Packard Model 5005A Signature Multimeter.

Dual Channel 100 MHz Oscilloscope with delta time measurement accurate to 0.5 ns. (Hewlett-Packard Model 1743A with probes or equivalent.)

1-13. DESCRIPTION.

1-14. The State Analyzer is used to monitor information flow in the data domain. The information may be a software program, the actions of a hardware state machine, or random logic signals.

1-15. The State Analyzer consists of one Model 64621A State Analysis Control Board, and from one to three State Data Acquisition Boards. The State Data Acquisition Boards may be the 40 Channel State Data Acquisition Board, the 20 Channel State Data Acquisition Board, or a combination of the two Acquisition Boards. The State Analyzer will have the necessary number of Data and Clock Probes for the Acquisition Boards used (Models 64635A and 64636A).

1-16. Up to three Acquisition Boards may be combined to form a State Analyzer with as many as 120 channels.

1-17. Logic Analyzers within one Mainframe may be connected together using the Inter Module Bus (IMB). One possible use of the IMB is to allow a State Analyzer to trigger a Timing Analyzer, or another State Analyzer.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64621A. Included are initial inspection procedures, preparation for use, and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

2-6. There are no specific preparation for use procedures except the actual installation of the boards in the Mainframe cardcage.

2-7. INSTALLATION INSTRUCTIONS.

2-8. MAINFRAME CONFIGURATION.

2-9. Depending on the number of channels required, the State Analysis Subsystem will use two or more card slots of the Mainframe cardcage.

2-10. Due to the way the Mainframe CPU identifies the boards installed in the cardcage, the State Control Board (64621A) should be installed in the lowest numbered card slot available.

2-11. The 64622A 40 Channel State Data Acquisition Boards (if any) must be installed in the next higher numbered card slots. See Figures 2-1 and 2-2.

2-12. The 64623A 20 Channel State Data Acquisition Board (if any) is installed in the next higher numbered slot. See Figures 2-1 and 2-2.

2-13. CARDCAGE SLOT IDENTIFICATION.

2-14. When the CPU finds a State Analysis Control Board in the cardcage, the CPU then expects to find either a 20 Channel Acquisition Board or a 40 Channel Acquisition Board in the next higher numbered slot.

2-15. The concept of the Control Board being in a lower numbered slot and Acquisition Boards in the higher slots is due to the system assigning labels (Pod 1, Pod 2, etc.) to the 20 bit groups of information stored in the Acquisition board's

memory. This is important when connecting the Pods to the User's System, and in Preprocessor applications (the software assumes that the information on Pod 1 is the Addresses from the User's System).

2-16. When connecting the Pod Cables to the State Analysis Boards, the Pods should be labeled as indicated in Figures 2-1 or 2-2, i.e., Pod 1 to Pod 1, etc.

2-17. Up to three Acquisition Boards may be installed with one Control Board forming one State Analysis Subsystem.

2-18. The State Analysis Subsystem configuration must not interfere with the Emulation Subsystem (if any) in the highest numbered card slots (some Mainframes may not have room for both a State Analysis Subsystem and an Emulation Subsystem).

2-19. SYNCHRONOUS EXPANSION BUS (SEB).

2-20. The State Control and Acquisition Boards must be grouped together to allow the Synchronous Expansion Bus (SEB) cable (W3) to connect the Control Board to the Acquisition Boards (J2). See Figures 2-1 and 2-2.

2-21. INTER MODULE BUS (IMB).

2-22. Some systems may contain more than one State Analysis Subsystem or a combination of a State Analyzer and another type of Analysis Subsystem. If this is the case, the second State Subsystem is installed in the same manner as the first one. If the second Analyzer is not a State Analyzer, refer to that Analyzer's Service Manual for installation information. The Inter Module Bus (IMB) Cable, W4, is installed accross the top of the boards (J1). See Figures 2-1 and 2-2.

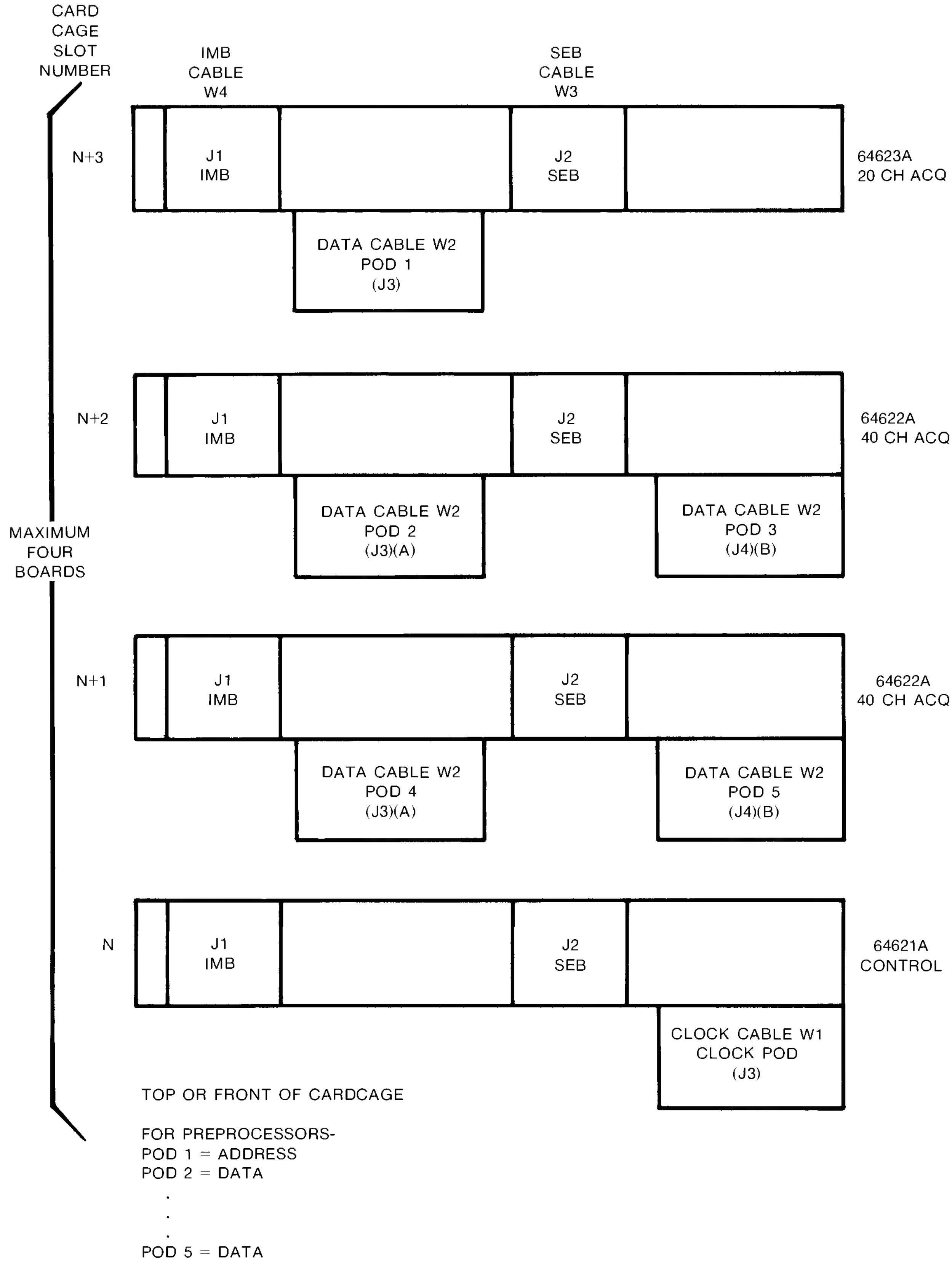


Figure 2-1. State Subsystem With 20 Channel Acquisition

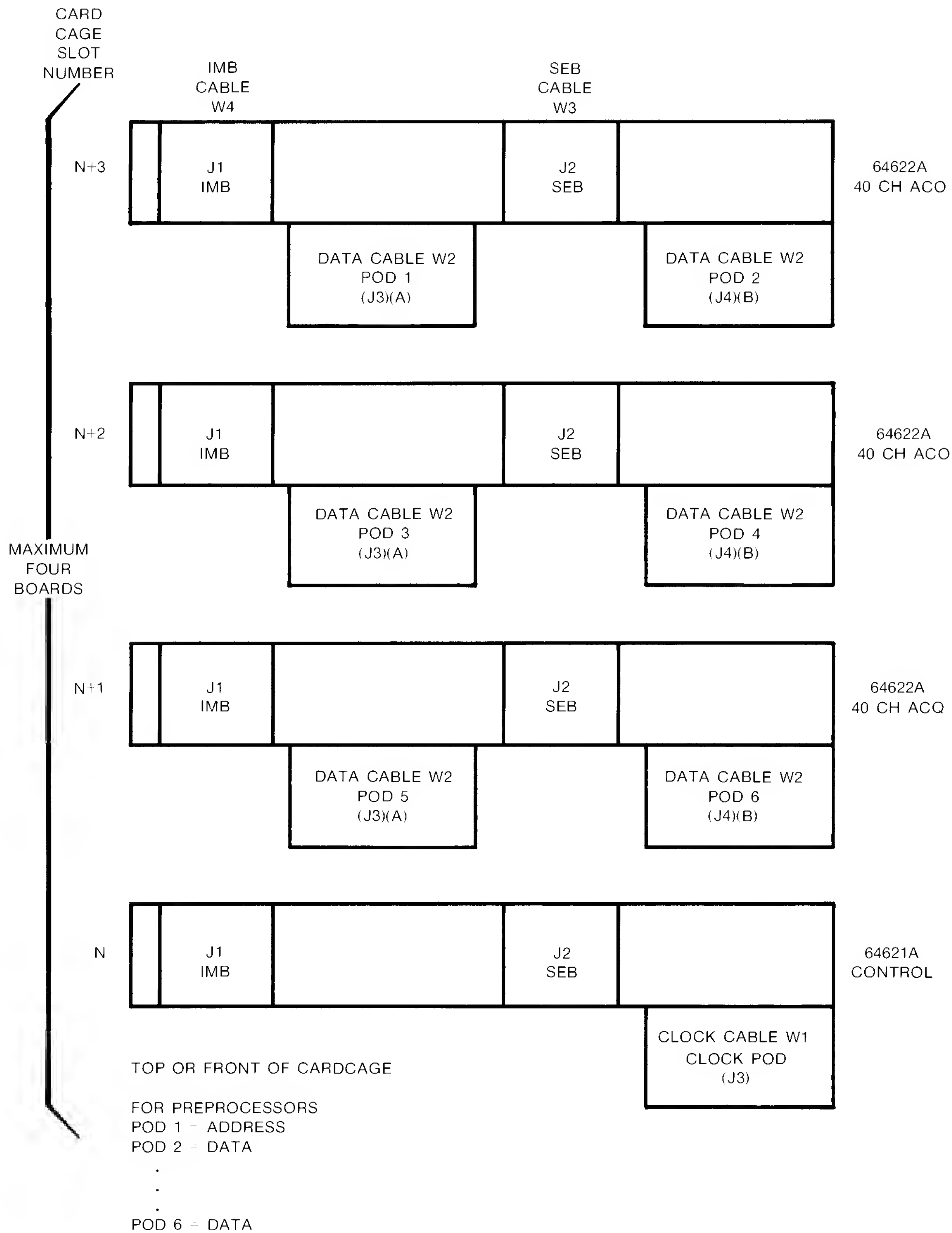


Figure 2-2. State Subsystem, No 20 Channel Acquisition

2-23. STORAGE AND SHIPMENT.

2-24. ENVIRONMENT.

2-25. This instrument may be stored or shipped in environments within the following limits:

Temperature.....................-40 Deg C to +75 Deg C
Humidity..................................5% to 80%
Altitude...........................15000 M (50000 ft)

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-26. PACKING.

2-27. Tagging for Service. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument repair number, and a description of the service required.

2-28. Original Packing. Containers and materials identical to those used in factory packing are available through Hewlett-Packard Offices. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and complete repair number.

2-29. Other Packing. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy plastic or paper. (If shipping to Hewlett-Packard Office or Service Center, attach a tag indicating type of service required, return address, model number, and complete repair number.

b. Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and complete repair number.

NOTES

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. The operation of the Model 64621A is a function of the system software. Complete operation from the keyboard of the system is beyond the scope of the Service Manual. Please refer to the Operator's Manuals for the procedure.

NOTES

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification (opt_test) for Model 64621A State Analysis Control Board. This Section consists of three parts; 1. Operation Verification, 2. Performance Verification, and 3. Troubleshooting.

4-3. The Operation Verification tests are all automatic and require no test equipment or dissassembly of the Mainframe. The Operation Verification provides a 90% assurance that the Model 64621A meets all specifications.

4-4. The Performance Verification tests require test equipment and disassembly of the Mainframe. The Performance Verification tests involve manual testing and verification of specifications. Therefore, the Performance Verification Tests should be run only by a qualified service person.

4-5. The Performance Verification tests are divided into two parts; 1. automated tests, and 2. manual tests. The automated test must all pass before performing the manual tests.

NOTE

> Before running the following tests, insure the boards are installed as indicated in Section II of this manual. Both Operation Tests and Performance Tests must be run to insure that the Model 64621A meets all specifications after repair.

4-6. The Troubleshooting portion of this Section describes the tests, shows the displays for the tests, decodes the displays, and tells how to use the tests with Signature Analysis for troubleshooting.

4-7. OPERATION VERIFICATION.

a. Press opt-test. RETURN.
b. Enter SLOT # of State Control Board. RETURN.
c. Press run all_boards. RETURN.
d. The status line near the bottom should read "STATUS: 10MHz Verification PASSED".
e. Run the continuity tests as outlined in Section IV of the Model 64635A General Purpose Data Probe, and the Model 64636A General Purpose Clock Probe Service Manuals.

4-8. PERFORMANCE VERIFICATION.

4-9. Automated Tests.

a. Press opt_test , RETURN.

b. Enter SLOT# of State Control Board , RETURN.

c. Press run all_boards , RETURN.

4-10. The status line near the bottom of the display should read "Status: 10MHz Verification Passed". If a failure occurred, refer to the paragraph on Troubleshooting in Section IV of this manual. This manual covers only the tests for the Control Board.

4-11. MANUAL TESTS.

4-12. TEST 1. INPUT THRESHOLD and MINIMUM SWING.

Refer to the Model 64635A and 64636A Service Manuals for the procedure.

4-13. TEST 2. INPUT THRESHOLD RANGE.

Refer to the Model 64635A and 64636A Service Manuals for the procedure.

4-14. TEST 3. MIN CLOCK WIDTH & QUAL SETUP & HOLD TIME.

Specifications:

Clock Width: 20 nS at threshold level.

Qualifier Setup Time: 20 nS.

Qualifier Hold Time: 0 nS.

Description:

This Test verifies that the clock input circuitry functions properly with an input signal having a minimum clock width.

Equipment:

Pulse Generator..........................HP8013B

Oscilloscope..................HP1722B or HP1743A

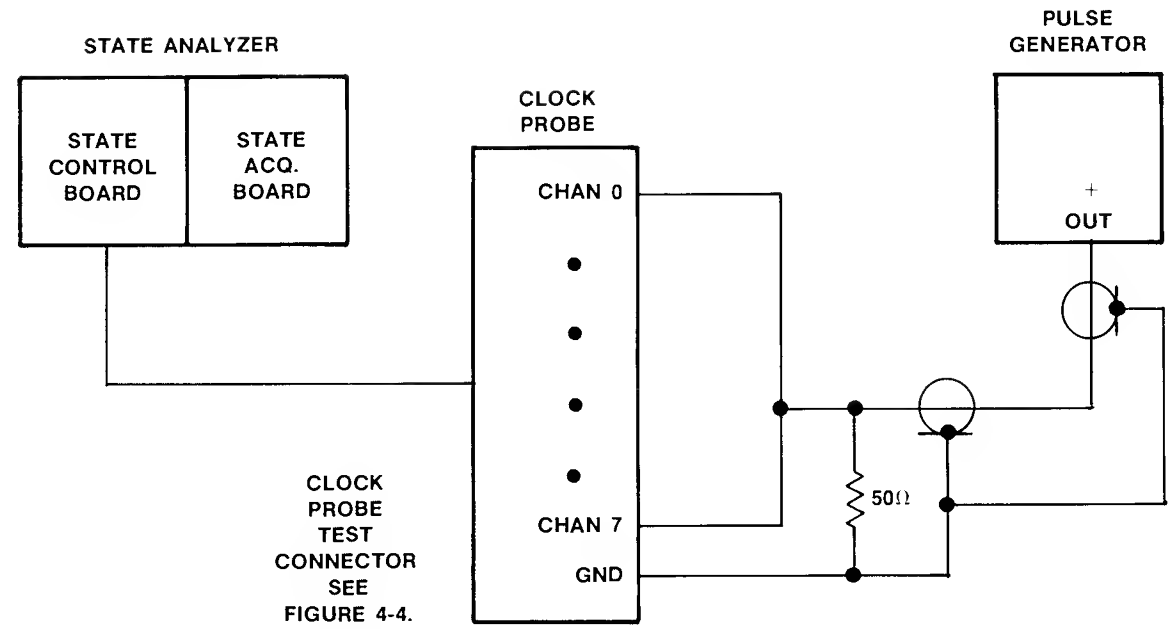


Figure 4-1. Clock Width Test Configuration

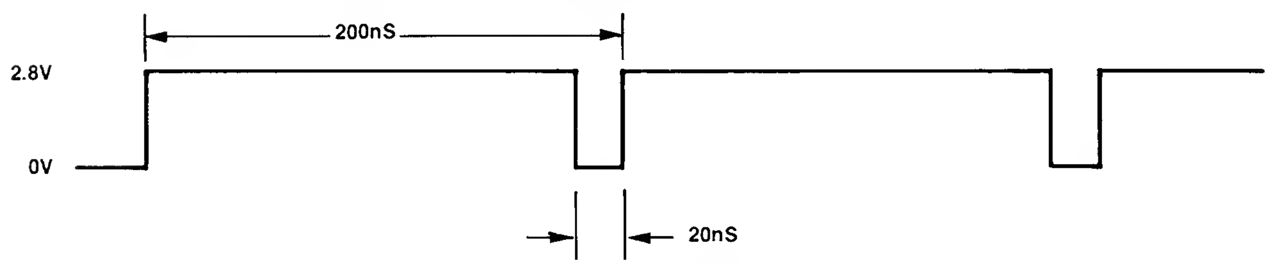


Figure 4-2. Clock Width Rising Edge Waveform

Procedure: (Need Control Board and at least one Acquisition Board with General Purpose Probes.)

a. Setup Pulse Generator for waveform in Figure 4-2.

b. Press meas_sys (only if more than one measurement system is installed).

c. Press state_x.

d. Press format_specification.

e. Press clock_is rising_edge channel_0 and low_level channel_1 and low_level channel_2 and .... low_level channel_7.

f. Press execute.

g. Verify on trace list that "time count rel" column is .16 uS, .20 uS, or .24 uS.

h. Repeat for rising edge of channel 1 through 7. Set all other clock channels to low level.

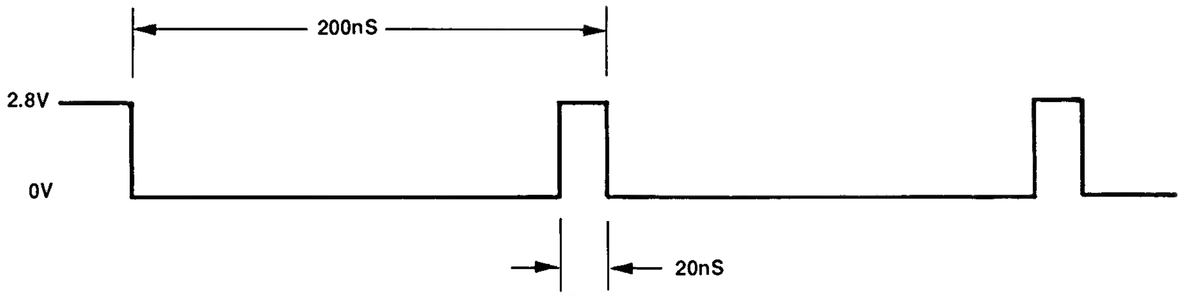


Figure 4-3. Clock Width Falling Edge Waveform

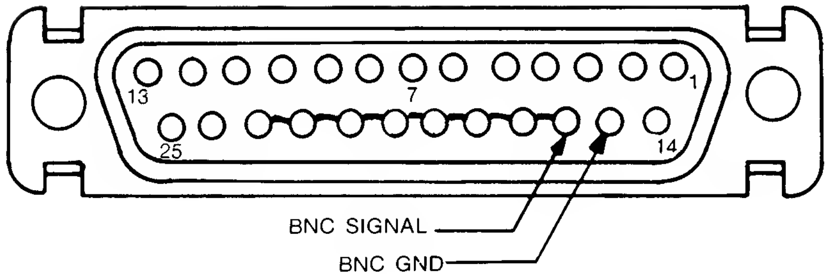
i. Setup Pulse Generator for the waveform in Figure 4-3.

j. Press clock_is falling_edge channel_0 and high_level channel_1 and high_level channel_2 and .... high_level channel_7.

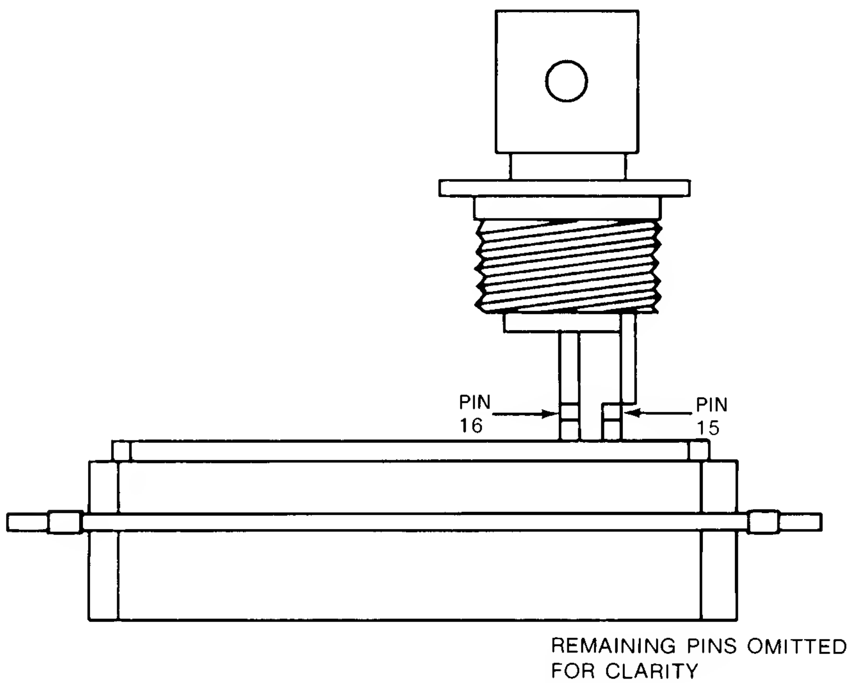
k. Press execute.

l. Verify on trace list that "time count rel" column is .16 uS, .20 uS, or .24 uS.

m. Repeat for falling edge of channel 1 through channel 7. Set all other clock channels to high level.



Jumper wire on RS232 connector. Signal on pins 16, 17, 18, 19, 20, 21, 22, and 23. Signal ground pin 15.



Connecting BNC to RS232 connector.

DBM-25P TRW cinch 1251-0063
BNC connector 1250-1032

Figure 4-4. Clock Probe Test Connector

4-15. TEST 4. DATA SETUP & HOLD TIME & QUAL CLOCK RATE.

Specifications:

Data Setup Time: 30 nS maximum.

Data Hold Time: 0 nS.

Description:

Since the data inputs are sampled with selected transitions of the clock, they must remain stable at the time of the clock to ensure that the desired input state is sampled. Data setup and hold time specifications define the time period that data inputs must remain stable. Data setup time is the time prior to the clock that data inputs must begin to be stable; data hold time is the time after the clock when data inputs are no longer required to remain stable. This test is to verify that the correct state is sampled when data inputs with minimum setup and hold time requirements are presented to the State Analyzer.

Equipment:

Pulse Generators (2).......................HP8013B

Oscilloscope...................HP1722B or HP1743A

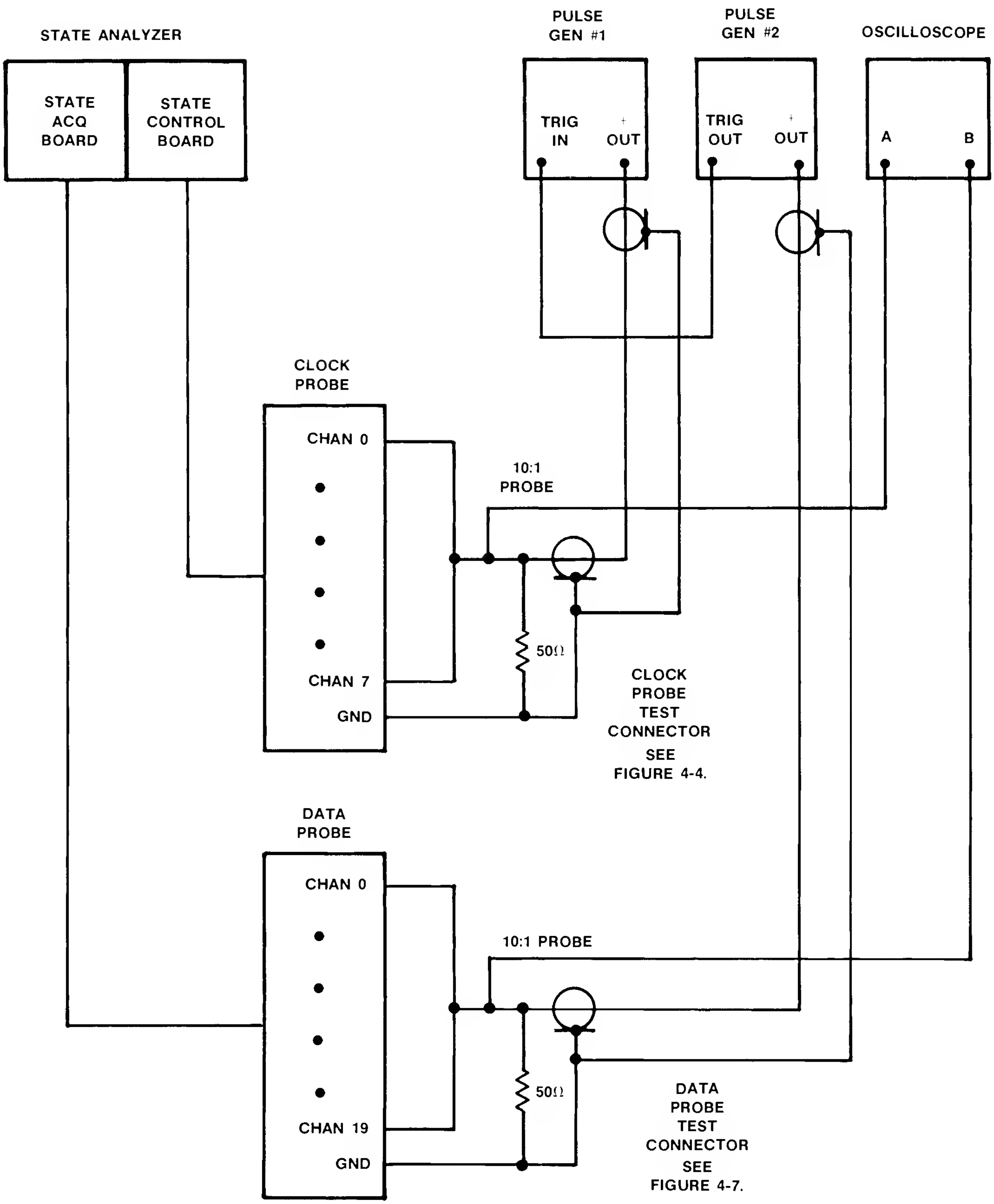


Figure 4-5. Setup and Hold Time Test Configuration

Procedure:

a. Press meas_sys (only if more than one measurement system is installed.)

b. Press state_x.

c. Press format_specification.

d. Adjust Pulse Generators 1 and 2 for waveforms A and B respectively as in Figure 4-6.

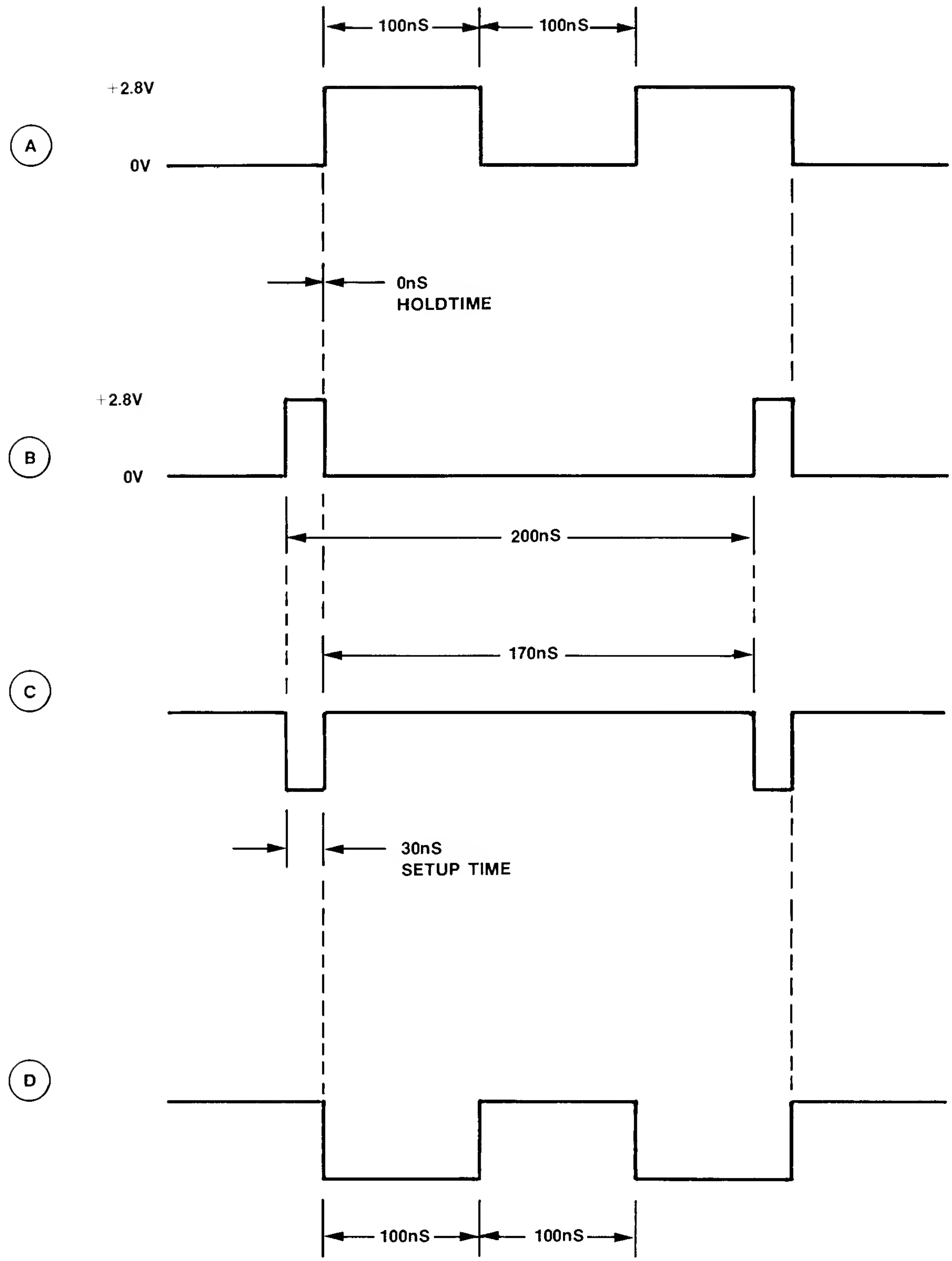


Figure 4-6. Setup and Hold Time Waveforms

e. Press execute.

f. Verify "11111H" for data probe under test.

g. Change Pulse Generator 2 to waveform C.

h. Press execute.

i. Verify "00000H" for data probe under test.

j. Change Pulse Generator 1 to waveform D.

k. Press format_specification.

l. Press clock_is falling_edge channel_0.

m. Press execute.

n. Verify "00000H" for data probe under test.

o. Change Pulse Generator 2 to waveform B.

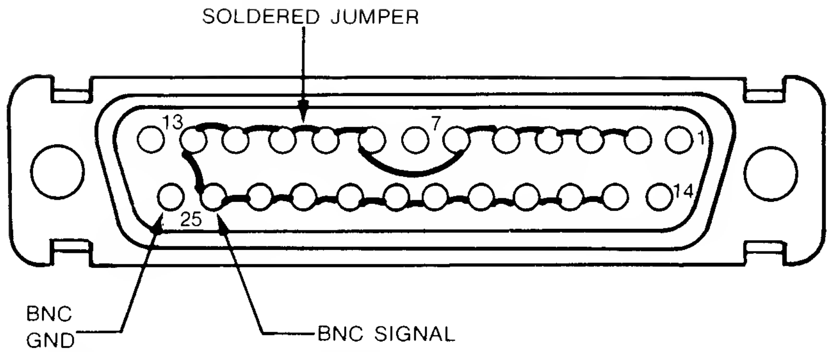
p. Press execute.

q. Verify "11111H" for data probe under test.

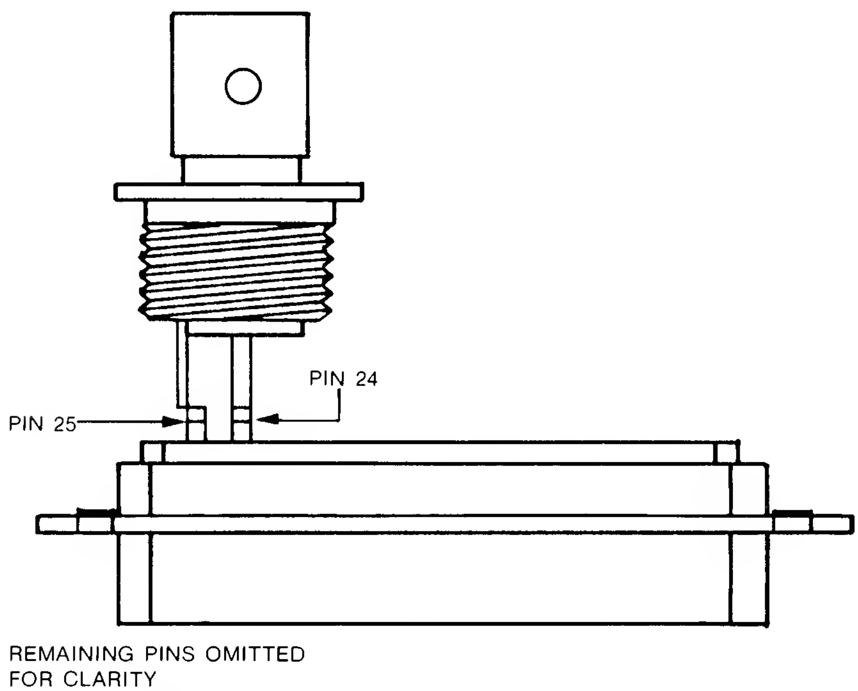
r. Press clock_is both_edges channel_0.

s. Press execute.

t. Verify alternating "00000H" and "11111H" for data probe under test and "time count rel" column is .08 uS or .12 uS.



Back view, looking at solder cups. Jumper wire on RS232 solder connector. Signal on pins 2-6, 8-12, 15-24. Signal ground on pin 25.



Side view, connecting BNC to RS232 connector.

DBM-25P TRW cinch 1251-0063
BNC connector 1250-1032

Figure 4-7. Data Probe Test Connector

4-16. TEST 5. BNC PORT OUTPUTS.

Specifications:

Stimulus (Port 1):

Pulse Width:

Trigger Events: 50 nS +/-20 nS.

Sequencer Events: 50 nS +/- 20 nS.

Delay From Clock:

Trigger Events: 225 nS +/-25 nS.

Sequencer Events: 200 nS +/-25 nS.

Halt (Port 2):

Delay From Clock:

Measurement Complete: 225 nS +/-25 nS.

Trace Point: 225 nS +/-25 nS.

Description :

Input clock, measure delay to BNCs using an Oscilloscope.

Equipment:

Pulse Generator............................HP8013B

Oscilloscope....................HP1722B or HP1743

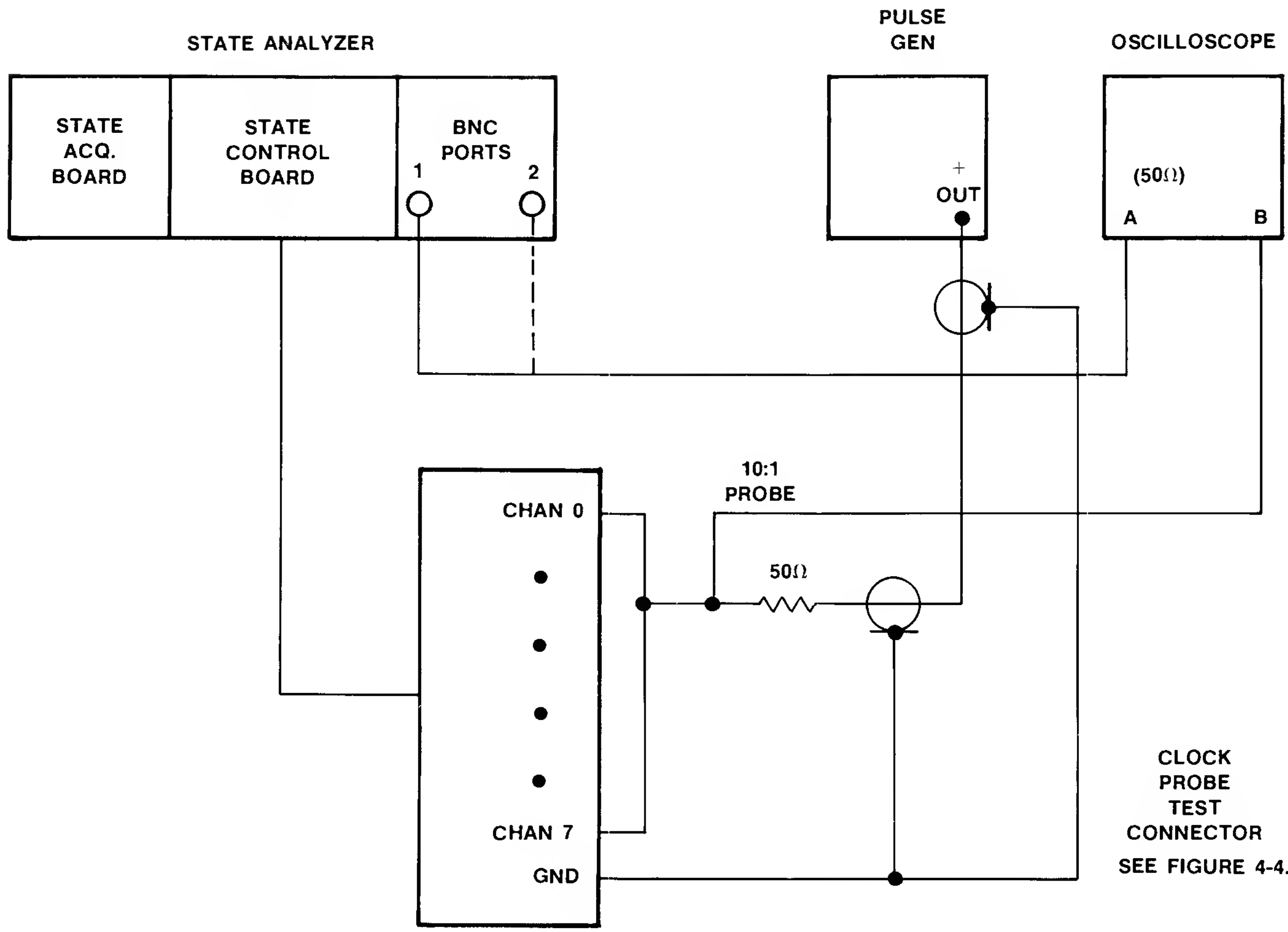


Figure 4-8. BNC Port Output Test Configuration

Procedure for Stimulus (BNC Port 1):

a. adjust Pulse Generator for 100 KHz (10 uS) square wave, with amplitude from 0 V. to +2.8 V. (Clock Threshold is automatically set for TTL = +1.4 V.)

b. Press meas_system (only if more than one measurement system is installed).

c. Press state_x.

d. Press assert bnc_port_1 on all_triggers.

e. Press execute repetitively.

f. Press trace_specification.

g. Set Oscilloscope to measure td and tw,as shown in Figure 4-9.

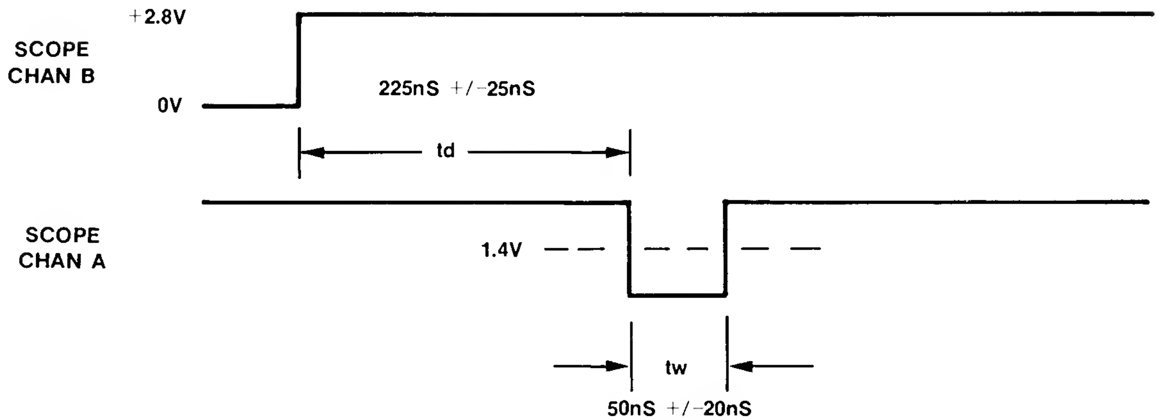


Figure 4-9. BNC Port 1 Waveform

h. Verify that Port 1 output for Trigger Events has a time delay (td) of 225 nS +/-25 nS, and a pulse width (tw) of 50 nS +/-20 nS measured at TTL levels (+1.4 V. threshold).

i. Press halt.

j. Press sequence term_number 1 find any_state enable.

k. Press sequence term_number 2 find any_state disable.

l. Press assert bnc_port_1 on sequence enable and disable.

m. Press trigger on nothing.

n. Press execute repetitively.

o. Press trace_specification.

p. Using the Pulse Generator set up of previous measurement, measure td and tw with the Oscilloscope.

q. Verify that Port 1 output for Sequence Events has a time delay (td) of 200 nS +/-25 nS and a pulse width (tw) of 50 nS +/- 20 nS measured at TTL levels (+1.4 V. threshold).

Procedure for Halt (BNC Port 2):

a. Move channel A of the Oscilloscope to Port 2.

b. Adjust Pulse Generator for square wave of 50 Hz with amplitude from 0 V. to +2.8 V. (Clock Threshold is automatically set for TTL = 1.4 V.)

c. Press halt.

d. Press trigger on any_state.

e. Press trigger position_is end_of_trace.

f. Press assert bnc_port_2 on measurement_complete.

g. Press execute repetitively.

h. Press trace_specification.

i. Set Oscilloscope to measure td. (Turn Intensity up to see channel A.)

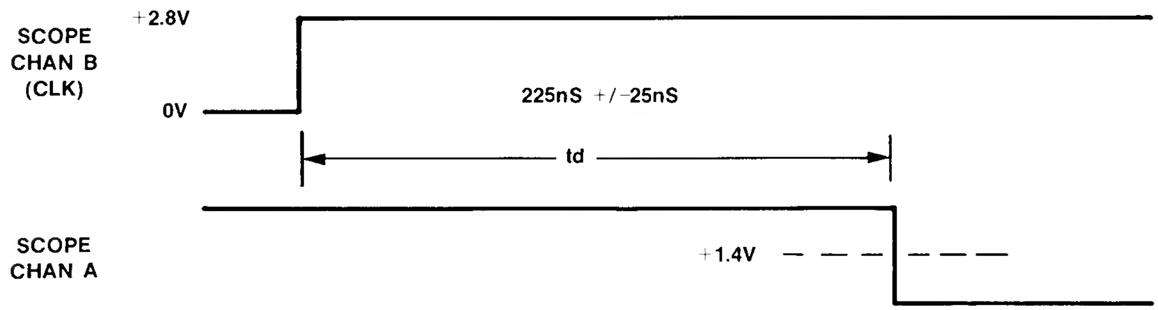


Figure 4-10. BNC Port 2 Waveform

j. Verify that Port 2 output for Measurement Complete has a time delay (td) of 225 nS +/-25 nS.

k. Press halt.

l. Press assert bnc_port_2 on trace_point.

m. Press execute repetitively.

n. Press trace_specification.

o. Using Oscilloscope set up of previous measurement, measure time delay (td).

p. Verify that Port 2 output for Trace Point has a time delay (td) of 225 nS +/-25 nS.

4-17. TROUBLESHOOTING.

4-18. General Comments. If the operation verification failed, troubleshoot the first test that failed, then re-run operational verification. The automatic tests listed in Figure 4-11 are interdependent so that all tests preceeding a given test must pass for the given test to pass.

```
10 MHz State Test: Board in Slot 2        Pass  Tested:  1   Failed:  0

    Test   Slot  2: State Control and Clock              Tested   Failed
  Automatic Tests
      1    Mainframe interface and stimulus                 1        0
      2    Control IC - shift register                      1        0
      3    Clock IC - shift register                        1        0
      4    Sequencer                                        1        0
      5    State count                                      1        0
      6    Trace memory                                     1        0
      7    Other counter tests                              1        0
      8    Intermodule Bus                                  1        0
  Manual Tests
      9    Strobe generator calibration                     0
     10    Threshold circuit calibration                    0
     11    Preproc interface data bus stimulus              0
     12    Rear panel PORT stimulus                         0
```

Figure 4-11. Automatic Tests

4-19. Tests 9 and 10 are used in Chapter V, Adjustments.

NOTE

> There are many TTL-ECL and ECL-TTL Translators in this product. A bad TTL level can be mistaken for a good ECL level! Please pay close attention to the levels when troubleshooting using the schematics. Also, a bad TTL input level can cause the entire TTL chip to output bad information.

4-20. Each automatic test is now described, and a signature analysis path provided. Each SA path works its way from the test output back towards the inputs. To run a particular test, press opt_test then RETURN. Press "SLOT #" of the State Control board, then RETURN. Finally, press run, "SLOT #", test, "test # (of first failing test)", repeat, then RETURN. Examples of valid commands while operating the State Analysis Performance verification are as follows:

a. "run 1 test 3 repeat RETURN". This runs test 3 repeatedly on the board in slot 1, and allows signatures to be taken.

b. "display 2 test 9 RETURN". This displays the results of test 9 for the board in slot 2. It does not cause test 9 to run. Various other commands are prompted by the softkeys, e.g., "stop" stops the test in progress; "list file_name" writes the display to the designated file; "end" causes the program to leave State Analysis PV and go to option_test PV.

4-21. When a bit pattern is given (e.g. data 00000100) the 1 indicates that bit 2 has failed. In all cases, a 0 indicates pass and a 1 indicates failure; the msb is to the extreme left; all patterns start with bit 0 unless otherwise noted.

4-22. The Synchronous Expansion Bus (SEB) connects the State Control board to State Acquisition boards. The SEB is not tested here; it is tested by the automatic tests for the State Acquisition boards. Also, the overview functions for the Analysis Controller chip are not tested here.

4-23. **Configuration.** For the purpose of running P.V. during fault isolation, the State Analysis Subsystem can be run in a minimum configuration. The minimum configuration for the various boards is shown in the following table:

Table 4-1. Troubleshooting Configurations

	Board Under Test		
Need	**64621A**	**64622A**	**64623A**
64621A	YES	YES	YES
64622A	NO	YES	YES
64623A	NO	NO	YES
Clock Probe	NO	NO	NO
Data Probe	N/A	NO	NO
SEB	NO	YES	YES
IMB	NO	NO	NO
Other Boards	NO	NO	NO

4-24. After repairing individual boards, the system must be configured to a standard configuration per Section II and pass the "run_all_boards" test. This will uncover system interaction problems or failures if they exist. Note that the IMB test using a Timing (64600S) Subsystem will pass only if the Timing Subsystem is completely installed and correctly cinfigured.

4-25. TEST 1: MAINFRAME INTRFC. and STIMULUS. LOOP A

4-26. Purpose -the purpose is two-fold, to verify that the mainframe can control the State Control board, and to stimulate the Sequencer and the Clock Threshold D/A Converters (DACs). The Strobe Generator is also exercised.

4-27. How -the Slow Clock Dectector is reset, then a Performance Verification Strobe (PPVSTB) is written to the Strobe Generator. This triggers the Slow Clock Detector monostable and its status is read at the Analysis Status Buffer.

4-28. Results -Strobe Request passes if the monostable is read high. Release data bus is a read of the mainframe data bus when nothing is addressed. Failure indicates that a card in the cardcage is causing problems on the data bus. The stimulus portion of this test is write only, therefore, no results are given for it.

```
10 MHz State Test: Board in Slot 2        Pass   Tested:  1   Failed:  0

  Slot  2: State Control and Clock
  Test  1: Mainframe interface and stimulus

  Strobe Request   Pass

  Release data bus 0000000000000000
```

Figure 4-12. Mainframe Interface

4-29. Stimulus -A staircase ramp is produced by the DACs (TP11 & TP12) during this test. See Figure 4-13. The DACs are also stimulated by test 10. The Sequencer is exercised in a write-only mode during this test in order to break its feedback loops. This test loads the Sequence Transition Memories and the Sequence Occurrence Counter Memories, then stimulates the Sequencer by operating the Sequence State Latch/Counter in the count mode (HLD asserted). Loopback occurs when the State Latch/Counter latch the next state from their parallel inputs (HLD is not asserted).

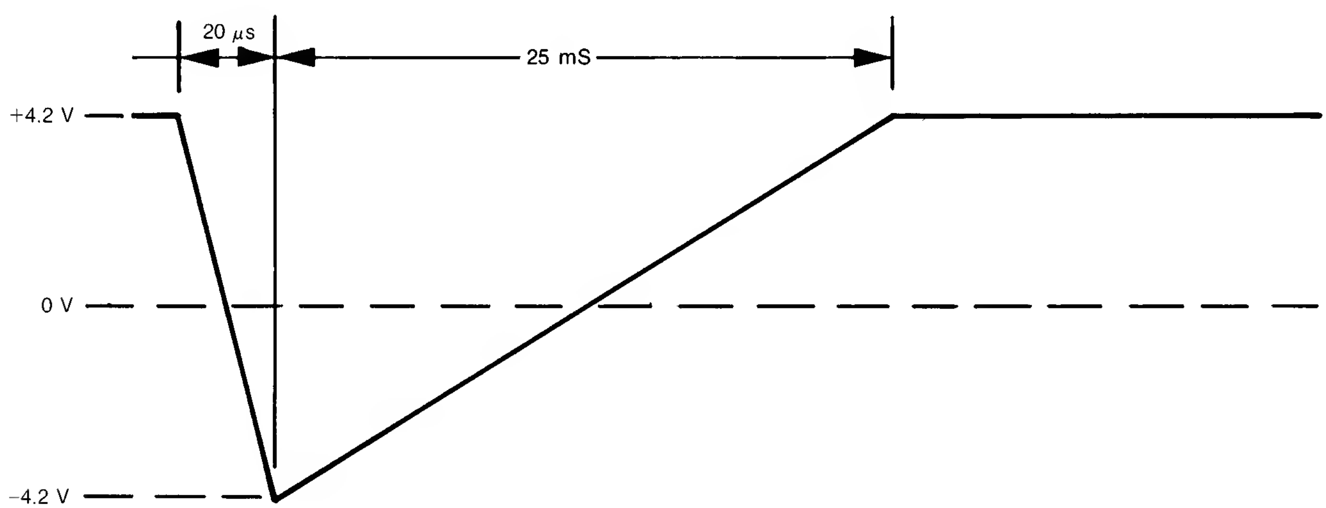


Figure 4-13. Stimulus

4-30. Loop A Signature Path for Strobe Request:U121, U122, U117, U65.

Loop A signature Path for Release Data Bus: U121, U122.

Loop A Signature Path for Strobe Generator: U24, U52, U8, U101.

Loop A Signature Path for DACs: U55, U54, U102, U121.

Loop A Signature Path for Sequencer: U16, U80, Occurrence Counter, Occurrence Count Memories, Transition Memories, Sequence State Latch/Counter, Mainframe Interface.

4-31. TEST 2: CONTROL IC - SHIFT REGISTER. LOOP B

4-32. Purpose - to verify that the shift register within the Analysis Controller, U1, can be loaded correctly.

4-33. How -Serial Data is loaded into U1 through pin 20. Pin 18 is the enable and pin 19 is the clock. Pin 17, NMC, outputs the same data 59 clock cycles later.

4-34. Results -Register data passes if the shift register overflowed correctly. The data is read by the Analysis Status Buffer as the signal NMC (memory complete). Shift control refers to the testing of the signal LLD.

```
10 MHz State Test: Board in Slot 2        Pass   Tested:  1    Failed:  0

  Slot  2: State Control and Clock
  Test  2: Control IC - shift register

 Register data
     All 0's    Pass
     All 1's    Pass
     Patterns   Pass

 Shift control  Pass

 NOTE: This tests only the shift register.
```

Figure 4-14. Control IC - Shift Register

4-35. Loop B Signature Path - U121, U122, U1, U103, U102.

4-36. TEST 3: CLOCK IC - SHIFT REGISTER. LOOP C

4-37. Purpose - to verify that the Clock Term Generator, U25, can be loaded correctly.

4-38. How - Serial Data is loaded into U25 pins 13 and 15. Pin 14 is the clock. Pins 26 and 28 output the same data several clock cycles later, and the results are read at the Status Buffer.

4-39. Results -Register input bits passes if the shift register overflowed correctly. The bits are read as HCD0 and HCD1 at the Analysis Status Buffer. External Clocks is an indirect test which shows that U25 is not activating the Strobe Generator.

```
10 MHz State Test: Board in Slot 2      Pass  Tested:  1    Failed:  0

  Slot  2: State Control and Clock
  Test  3: Clock IC - shift register

 Register input bits  10

      All 0's         00   (1 = Error)

      All 1's         00

      Patterns        00

 External Clocks      Pass
```

Figure 4-15. Clock IC - Shift Register

4-40. Loop C Signature Path - U121, U122, U25, U102.

4-41. TEST 4: SEQUENCER. LOOP D

4-42. Purpose - to verify operation of the Sequencer.

NOTE

> This test contains two feedback loops -U16 pin 3 to U17 pin 11 (LOCCRY) and U42 outputs to U18 parallel inputs. Signature Analysis of feedback loops might fail to isolate the failed component. In that case, use Test 1 which stimulates the Sequencer without allowing loopback. Also, all locations of the Sequence Transition Memories are not tested. If a Transition Memory failure is suspected, use Test 1 because it exercises all memory locations.

4-43. How -With the Sequence State Latch/Counter in the count (load) mode, Transition Memories and the Occurrence Memories are loaded. The Analysis Controller and the Sequence State Latch/Counter are then put into the run mode, and strobes are generated via PPVSTB. The events that follow are complex and only an overview is given here. The Sequence State Latch/Counter is clocked by PPLS (pipeline strobe) which is enabled by the Analysis Controller at U5. The Sequence State is the output of the Sequence State Latch/Counter, and is read as TSS0-7 (Trace Sequence State) by the Sequence Read Register.

4-44. Next, the Sequence Occurrence Counter and Counter Memories are tested. The Counter is clocked by PSOCINC. PSOCINC in the run mode is enabled by the Analysis Controller at U5. The only output of the Occurrence Counter is Occurrence Carry (LOCCRY) it is latched by the Pipeline Latch/Counter and read as TSS4, using the Sequence Read Register. RAM address in Figure 4-16 refers to the output of U42; it is also latched by the Pipeline Latch/Counter and then read as TSS4-7 by the Sequence Read Register.

4-45. Now the plot thickens. The Trace Count/Status Memory Address Counter (MAC) and Trace Point bit (LTRCP) are needed to test the outputs of memories U36 and U38 which are processed by the Analysis Controller. The MAC is cleared, incremented by HQWRITE, and read by the Trace MAC Read Register; Figure 4-16 reports this as Memory Address. Trace Point is tested by clearing U98, then setting it by having the Analysis Controller issue an NTRIG (Trigger). The result, LTRCP, is read by the Analysis Status Buffer.

4-46. Sequence Addressing in Figure 4-16 is a test of the address lines of the Transition Memories. RAM U36 and the Analysis Controller are loaded so that a walking ones address pattern causes U36 to output Sequence Store Qualify (LSSQ). This causes the Analysis Controller to enable HQWRT, provided other Analysis Controller inputs are good. Also, HBOTF can cause failures in HSTR signal. HQWRT increments the MAC. Now that the Transition Memories and the MAC and LTRCP are known to work, additional functions of the Analysis Controller can be tested. The Analysis Controller inputs tested are HSTR (Sequencer Trigger), LSTE (Sequencer Trigger Enable), LSSE (Sequencer Store Enable), and LSME (Sequencer Master Enable). The results are obtained from the NTRIG and HQWRITE outputs of the Analysis Controller.

4-47. Results - all results of this test are read at one of three places: the Sequence Read Register, the Trace MAC Read Register, or LTRCP at the Analysis Status Buffer.

```
10 MHz State Test: Board in Slot 2        Pass  Tested:  1   Failed:  0

  Slot  2: State Control and Clock
  Test  4: Sequencer

                                 54321_9876543210
 State Register Count                    00000000
                Load                     00000000

 Occur Counter Bits True         0000000000000000
                    False        0000000000000000
               RAM Address                   0000

 Memory Address                          00000000, Trace Point Pass

 Sequence Addressing                         Pass
          Functions                          0000 (HSTR,LSTE,LSSE,LSME)
```

Figure 4-16. Sequencer

4-48. Figure 4-16 Interpretation.

State Register Count 00000000
(eight bit Sequence State output by U17 and U18 when clocked by NINCSS)

Load 00000000
(eight bit Sequence State latched by U17 and U18 when HLD is not asserted)

Occur Counter Bits True 0000000000000000 *(No Carry Load)
False 0000000000000000
(sixteen bits loaded from U58-U61 into U78,U79,U81,U82, then unloaded through each pin 4 and gated by U80 and U16 to become LOCCRY)

RAM Address 0000
(four bit input to U58-U61 on lines A0-A3)

Memory Address 00000000, Trace Point Pass
(outputs of U104 and U105 read at U68, Trace Point is the output of U98 read at U122)

Sequence Addressing Pass
(bits A0-A7 of U36 tested by output at pin 4, LSSQ)

Functions 0000 (HSTR,LSTE,LSSE,LSME)
(U1 input pins 2,37,36,38 tested at U1 output pins 4,35)

* appears on failure of c arry bit on U78 pin 4 only.

4-49. Loop D Signature Path for State Register: U121, U89, U83, U84, U17, U18, U85, U52, U101.

Loop D Signature Path for Occurrence Counter: U16, U78-U82, U58-U61, U42, U62-U64, U17, U18. (Note: go to Test 1 for test without loopback)

Loop D Signature Path for Memory Address: U121, U122, U68, U98, U104, U105, U5, U1.

Loop D Signature Path for Sequence Addressing and Functions:U1, U36, U38.

4-50. TEST 5: STATE COUNT. LOOP E

4-51. Purpose - verify operation of the Trace State/Time Counter U112 in the state count mode.

4-52. How -The Counter temporarily stores data in location 00(Hex) of the Trace Count/Status Memory. That location is read at the Trace Data Read Register.

4-53. One difficulity with this test is that it requires the Trace Count/Status Memory to work before it is tested (Test 6). In particular, the address used to write data to the RAMs is not sampled in Test 5 because RAM outputs are sampled at read time. If Test 5 fails and only RAM outputs are bad, test the Trace Count/Status Memory Address Selector and the Memory Address Counter using signature analysis, or run Test 6 and take signatures in both the main loop and the write loop.

4-54. The Counter uses the following controls: HQWRT which resets the Counter; PINC which increments the count states; LSTATE which puts the Counter in the count states mode; HCTST which selects between a 20 bit mode and two 10 bit modes; HCQ which enables the Counter; and 25MHz which is used internally by the Counter.

4-55. Results -all results for this test are read by the Trace Data Read Register. That register receives data from the memory bank selected by the signals LTCSMS0-3 (Low Trace Count/Status Memory Select). U70, U73 and U90 are not used by this test.

```
10 MHz State Test: Board in Slot 2        Pass Tested:  1   Failed:  0

  Slot  2: State Control and Clock
  Test  5: State count

                   98765432109876543210
  Reset to 0       00000000000000000000     (1 = Error)

  Count enable     Pass

  10/10  count     Pass

  20 bit count     Pass

  Output test
     0's           00000000000000000000
     1's           00000000000000000000
```

Figure 4-17. State Count

4-56. Figure 4-17 Interpretation.

```
Reset to 0     00000000000000000000
   (twenty output bits of U112 read from memory: b19 - b16 = U93
                                                 b15 - b12 = U72
                                                 b11 - b8  = U92
                                                 b7  - b4  = U71
                                                 b3  - b0  = U91
Count enable     Pass
   (test of HCOUNTQUAL)
10/10  count     Pass
   (two ten bit counter mode, selected by HCTST)
20 bit count     Pass (20 bit counter mode)
Output test
   0's         00000000000000000000
   1's         00000000000000000000
   (same outputs as Reset to 0 above)
```

4-57. Loop E Signature Path: U69, U87, U88, U104, U105, U106, memory RAM's, ECL/TTL translators, U112, U1, U120, U100, U102.

4-58. TEST 6: TRACE MEMORY. LOOPS F & G

4-59. Purpose -test Trace Counter/Status Memory, Tracepoint Register, Wrap bit, and Post Trace Point Counter which is a circuit internal to the Analysis Controller.

4-60. How -The Memory is 32 bits wide. 20 bits are Counter data, 8 bits are Sequence State data and the remaining 4 bits are for flags. In addition to the RAMs, the Memory contains an Address Counter (MAC), and an Address Selector. The MAC can be read through the Tracepoint Register and the Trace MAC Read Register.

461. Write Loop. The main loop, loop F, of this test takes signatures when the RAMs are being read, and while the RAM addresses are being selected from the CPU via U86 and a high on the select line of the Trace Count/Status Memoery Address selector. The write loop, loop G, allows the RAM addresses to be tested when the Memory Address Counter is selected.

4-62. Previous tests have verified the functioning of the MAC and its associated Trace MAC Read Register. Test 5 used the Address Selector and location 00 Hex of the memory. Therefore, the most likely failures detected by this test are the remaining memory locations, particularly U70, U73, and U90 which were not tested in Test 5.

4-63. Other circuitry tested for the first time include U67 Tracepoint Register, U98 -Wrap bit, and Post Trace Point Counter function of U1.

4-64. Results - all testing results are read at the Analysis Status Buffer U122 and the CPU Data Buffer U121.

```
10 MHz State Test: Board in Slot 2        Pass  Tested:  1   Failed:  0

  Slot  2: State Control and Clock
  Test  6: Trace memory

   (1 = Error)            Address Bit              Memory Channel
                           76543210     10987654321098765432109876543210

 Address Counter           00000000
 Trace Point Reg           00000000
 Trace Point, Wrap               00
 Store seq state                                                00000000
       mostly 1's                       00000000000000000000000000000000
       mostly 0's                       00000000000000000000000000000000
 Address Test              00000000     00000000000000000000000000000000

 Index Counter             Pass
```

Figure 4-18. Trace Memory

4-65. Figure 4-18 Interpretation.

Address Counter	00000000	
(outputs of U104 and U105 read at U68)		
Trace Point Reg	00000000	
(U67)		
Trace Point, Wrap	00	
(U98 pin 7 and U103 pin 9 respectively)		
Store seq state		00000000
mostly 1's		000000000000000000000000000000
mostly 0's		000000000000000000000000000000
Address Test	00000000	000000000000000000000000000000
(indirect test of RAM address bits A0-A7)		
*Index Counter	Pass	
(strobe inputs to U1 cause counter to overflow at U1 pin 17)		

(32 bit memory read at U69. Bit pattern:
b31 - b28 = U71
b27 - b24 = U91
b23 - b20 = U72
b19 - b16 = U92
b15 - b12 = U73
b11 - b8 = U93
b7 - b4 = U70
b3 - b0 = U90

*The Index Counter is shown as the Post Trace Point Counter on the Block Diagram.

4-66. Loop F Signature Path:U121, U122, U67-U69, U98, U103-U105, U86-U88.

Loop F signature Path for Trace Count/Status Memory: U112, U1.

4-67. TEST 7: OTHER COUNTER TESTS.

4-68. Purpose - verify operation of prescale function and count time mode of Trace State/Time Counter.

4-69. How - The Counter is incremented by the 25 MHz clock and the count is stored in the Trace Count/Status Memory location 00 Hex.

4-70. Results - Signature Analyis is impractical because the interval is greater than 9 seconds. The only untested signals are HTIMS and LSTATE. HTIMS is a Strobe Generator output. LSTATE should oscillate. If all other tests pass, replace the Counter, U112, and rerun the test.

```
10 MHz State Test: Board in Slot 2        Pass  Tested:  1   Failed:  0

   Slot  2: State Control and Clock
   Test  7: Other counter tests

   Prescale 1  Pass

            2  Pass

            3  Pass

   Time enable Pass

   Time reset  Pass

   Prescale 4  Pass
```

Figure 4-19. Other Counter Tests

4-71. TEST 8: INTERMODULE BUS.

4-72. This test has two parts: internal test using loopback in the Analysis Controller, and external test which requires that another system be connected via the Intermodule Bus (IMB).

4-73. Assuming all cables, connections and configurations are correct and working properly, failure of this test indicates that the Analysis Controller of one of the systems is failing. If no external system is connected, the test will still indicate pass, provided the internal test passes.

4-74. The State Analysis PV software provides the test IMB softkey for IMB testing. It selects the board that is to be the Intermodule Bus Driver.

```
10 MHz State Test: Board in Slot 3        Pass   Tested:  1    Failed:  0

   Slot  3: State Control and Clock
   Test  8: Intermodule Bus

   Internal tests
        Master Enable   Pass
        Trigger Enable  Pass
        Storage Enable  Pass

   Tests with IMB test board  No IMB test board               (1 = Error)
        Receive               (ME,TE,SE,TR)
        Drive                 (Port1 pulses,DClk,Port2,Port1,ME,TE,SE,TR)

   IMB test board limitations                           (1 = Not tested)
        Drive                 (ME,TE,SE,TR)
        Receive               (Port1 pulses,DClk,Port2,Port1,ME,TE,SE,TR)
```

Figure 4-20. Intermodule Bus

4-75. TEST 9: STROBE GENERATOR CALIBRATION.

4-76. This test is a stimulus to the Control Board only. It is used in Section V for calibration of the Strobe Generator. See Section V.

4-77. TEST 10: THRESHOLD CIRCUIT CALIBRATION.

4-78. This test is a stimulus to the Control Board only. It is used in Section V for calibration of the Threshold Circuit. See Section V.

4-79. TEST 11: PREPROCESSOR INTRFC. STIMULUS. LOOP H

4-80. Purpose - to verify that the Control Board can write to the Preprocessor. No data is read from the Preprocessor.

4-81. How -When LMS is activated, the address and data information on the CPU bus is loaded into U26 and U53 and read at the outputs of U26 and U53. At the same time the control signals are read at the outputs of U129.

4-82. Results - All results of this test are read at the Address Latch U118, or the CPU Data Buffer U121.

483. Loop H Signature Paths:

U26, U118, U127, U53

U1, U123, U65, U116, U96, U119, U127, U120, U99, U129.

4-84. TEST 12: REAR PANEL PORT STIMULUS. LOOP I

485. Purpose - to verify that the control board writes to PORT1 and PORT2 on the rear panel of the Mainframe.

486. How - there are two sections to this test:

1. The PHALT signal is activated and sent to BNC2 when the control signal, PWRUN, goes high. This latches LAB1, Low Address Bus 1, into the Port Latches (U97).

2. The PSTIM signal is activated and sent to PORT1 when NTRIG, Negative Trigger, from U1 goes low. This occurrs each time the trigger event is encountered.

4-87. Loop I Signature Path:

U1, U97, U123, U116, U126.

Board # 64621-66503 **Test 1: Loop A - VH = 8U24**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

```
U  1- 7  PH15   ECL
U  1-30  PH15   ECL
U  1-36  PH15   ECL
U  1-37  4778   ECL
U  1-38  4778   ECL
U  1-39  high   ECL
U  1-40  4778   ECL

U  6- 3  72C0   ECL
U  6- 6  UH94   ECL
U  6- 7  0000   ECL
TOTLZ = 1
U  6- 9  8HF9   ECL
U  6-12  0000   ECL
U  6-13  8HF9   ECL

U  8- 1  UF8C
U  8- 2  UF8C
U  8- 3  73AU
U  8- 4  73AU
U  8- 5  73AU
U  8- 6  UF8C

U 16- 3  18F3   ECL
U 16- 6  0965   ECL
U 16- 7  P4F6   ECL

U 17- 2  03P7   ECL
U 17- 3  C427   ECL
U 17- 4  1A92   ECL
U 17- 5  high   ECL
U 17- 6  low    ECL
U 17- 7  low    ECL
U 17- 9  low    ECL
U 17-10  high   ECL
U 17-11  18F3   ECL
U 17-12  22F4   ECL
U 17-13  PP34   ECL
U 17-14  F61U   ECL
U 17-15  78AA   ECL

U 18- 2  62FC   ECL
U 18- 3  65A6   ECL
U 18- 5  high   ECL
U 18- 6  1A92   ECL
U 18- 7  7FCH   ECL
U 18- 9  9946   ECL
U 18-10  082C   ECL
U 18-11  PHAC   ECL
U 18-12  22F4   ECL
U 18-13  PP34   ECL
U 18-14  762F   ECL
U 18-15  H02H   ECL

U 19- 9  1A92   ECL
U 19-11  080P   ECL
U 19-12  low    ECL
U 19-14  PCH0   ECL
U 19-15  high   ECL

U 20- 9  8U24   ECL
U 20-10  0000   ECL
TOTLZ = 1
U 20-11  0000   ECL
TOTLZ = 1
U 20-12  8U24   ECL
TOTLZ = 1
U 20-13  0000   ECL
TOTLZ = 1
U 20-14  8U24   ECL
U 20-15  0000   ECL

U 21- 2  0000   ECL
U 21- 3  8U24   ECL
U 21- 4  0000   ECL
TOTLZ = 1
U 21- 6  0000   ECL
TOTLZ = 1
U 21- 7  0000   ECL
TOTLZ = 1

U 21-10  0000   ECL
TOTLZ = 1
U 21-11  0000   ECL
TOTLZ = 1
U 21-13  0000   ECL
TOTLZ = 1
U 21-14  8U24   ECL
TOTLZ = 1
U 21-15  0000   ECL

U 22- 2  0000   ECL
U 22- 3  8U24   ECL
U 22- 4  0000   ECL
TOTLZ = 1
U 22- 6  0000   ECL
TOTLZ = 1
U 22- 7  0000   ECL
TOTLZ = 1
U 22-10  0000   ECL
TOTLZ = 1
U 22-11  0000   ECL
TOTLZ = 1
U 22-13  0000   ECL
TOTLZ = 1
U 22-14  8U24   ECL
U 22-15  0000   ECL

U 23- 2  0000   ECL
U 23- 3  8U24   ECL
U 23- 4  0000   ECL
TOTLZ = 1
U 23- 6  0000   ECL
TOTLZ = 1
U 23- 7  high   ECL
TOTLZ = 1
U 23-10  high   ECL
U 23-11  73AU   ECL
U 23-13  0000   ECL
U 23-14  8U24   ECL
TOTLZ = 1
U 23-15  0000   ECL
```

Board # 64621-66503

Test 1: Loop A - VH = 8U24

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 24- 2	73AU	ECL
U 24- 4	73AU	ECL
U 24- 5	high	ECL
U 25-13	508P	
U 25-15	6302	
U 26-19	8U24	
TOTLZ = 0		
U 36- 2	4778	ECL
U 36- 4	PH15	ECL
U 36- 6	A59P	ECL
U 36- 7	4871	ECL
U 36- 8	9U0H	ECL
U 36- 9	62FC	ECL
U 36-10	H02H	ECL
U 36-11	762F	ECL
U 36-13	C427	ECL
U 36-14	03P7	ECL
U 36-15	78AA	ECL
U 36-16	165A	ECL
U 36-17	65A6	ECL
U 36-18	8PC9	ECL
U 36-19	048C	ECL
U 36-21	9U0H	ECL
U 36-23	PCH0	ECL
U 38- 2	4778	ECL
U 38- 4	PH15	ECL
U 38- 6	508P	ECL
U 38- 7	6302	ECL
U 38- 8	9U0H	ECL
U 38- 9	62FC	ECL
U 38-10	H02H	ECL
U 38-11	762F	ECL
U 38-13	C427	ECL
U 38-14	03P7	ECL

U 38-15	78AA	ECL
U 38-16	F61U	ECL
U 38-17	65A6	ECL
U 38-18	99F7	ECL
U 38-19	357P	ECL
U 38-21	4778	ECL
U 38-23	PH15	ECL
U 40- 2	PPHP	ECL
U 40- 4	5HA1	ECL
U 40- 6	A59P	ECL
U 40- 7	4871	ECL
U 40- 8	FFU9	ECL
U 40- 9	62FC	ECL
U 40-10	H02H	ECL
U 40-11	762F	ECL
U 40-13	C427	ECL
U 40-14	03P7	ECL
U 40-15	78AA	ECL
U 40-16	F61U	ECL
U 40-17	65A6	ECL
U 40-18	P14U	ECL
U 40-19	048C	ECL
U 40-21	8HF9	ECL
U 40-23	UH94	ECL
U 42- 2	7FCH	ECL
U 42- 4	9946	ECL
U 42- 6	508P	ECL
U 42- 7	6302	ECL
U 42- 8	FFU9	ECL
U 42- 9	62FC	ECL
U 42-10	H02H	ECL
U 42-11	762F	ECL
U 42-13	C427	ECL
U 42-14	03P7	ECL
U 42-15	78AA	ECL
U 42-16	F61U	ECL
U 42-17	65A6	ECL
U 42-18	99F7	ECL
U 42-19	357P	ECL
U 42-21	082C	ECL
U 42-23	PHAC	ECL

U 52- 5	73AU	
U 52- 7	high	
U 52-10	high	
U 52- 1	high	ECL
U 52- 2	73AU	ECL
U 52- 3	low	ECL
U 52- 4	high	ECL
U 52-12	73AU	ECL
U 52-15	high	ECL
U 54- 2	048C	
U 54- 3	8PC9	
U 54- 4	4871	
U 54- 5	A59P	
U 54- 6	357P	
U 54- 7	99F7	
U 54- 8	6302	
U 54- 9	508P	
U 54-12	2FF1	
U 55- 2	048C	
U 55- 3	8PC9	
U 55- 4	4871	
U 55- 5	A59P	
U 55- 6	357P	
U 55- 7	99F7	
U 55- 8	6302	
U 55- 9	508P	
U 55-12	9153	
U 58- 1	1C85	ECL
U 58- 2	42C2	ECL
U 58- 4	4871	ECL
U 58- 5	A59P	ECL
U 58- 6	PHAC	ECL
U 58- 7	082C	ECL
U 58- 9	9946	ECL

Model 64621A - Performance Verification

Board # 64621-66503

Test 1: Loop A - VH = 8U24

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 58-10	7FCH	ECL
U 58-11	8PC9	ECL
U 58-12	048C	ECL
U 58-13	5A59	ECL
U 58-14	1C85	ECL
U 58-15	42C2	ECL
U 59- 1	U5C3	ECL
U 59- 2	PFH9	ECL
U 59- 4	4871	ECL
U 59- 5	A59P	ECL
U 59- 6	PHAC	ECL
U 59- 7	082C	ECL
U 59- 9	9946	ECL
U 59-10	7FCH	ECL
U 59-11	8PC9	ECL
U 59-12	048C	ECL
U 59-13	25HU	ECL
U 59-14	U5C3	ECL
U 60- 1	1C85	ECL
U 60- 4	6302	ECL
U 60- 5	508P	ECL
U 60- 6	PHAC	ECL
U 60- 7	082C	ECL
U 60- 9	9946	ECL
U 60-10	7FCH	ECL
U 60-11	99F7	ECL
U 60-12	357P	ECL
U 60-13	5A59	ECL
U 60-14	1C85	ECL
U 60-15	42C2	ECL
U 61- 1	U5C3	ECL
U 61- 2	PFH9	ECL
U 61- 4	6302	ECL
U 61- 5	508P	ECL
U 61- 6	PHAC	ECL
U 61- 7	082C	ECL
U 61- 9	9946	ECL
U 61-10	7FCH	ECL
U 61-11	99F7	ECL
U 61-12	357P	ECL
U 61-13	25HU	ECL
U 61-14	U5C3	ECL
U 61-15	PFH9	ECL
U 62- 5	FFU9	
U 62- 7	9U0H	
U 62-10	5A59	
U 62-11	25HU	
U 62- 1	9U0H	ECL
U 62- 2	FFU9	ECL
U 62-14	25HU	ECL
U 62-15	5A59	ECL
U 63- 5	508P	
U 63- 7	6302	
U 63-10	357P	
U 63-11	99F7	
U 63- 1	6302	ECL
U 63- 2	508P	ECL
U 63-14	99F7	ECL
U 63-15	357P	ECL
U 64- 5	A59P	
U 64- 7	4871	
U 64-10	048C	
U 64-11	8PC9	
U 64- 1	4871	ECL
U 64- 2	A59P	ECL
U 64-14	8PC9	ECL
U 64-15	048C	ECL
U 65-13	0000	

TOTLZ = 1

U 67- 1	high	
U 68- 1	high	
U 69- 1	high	
U 78- 4	0965	ECL
U 78- 5	PPHP	ECL
U 78- 6	P4F6	ECL
U 78- 7	42C2	ECL
U 78- 9	1C85	ECL
U 78-10	42C2	ECL
U 78-11	1C85	ECL
U 78-12	low	ECL
U 78-13	080P	ECL
U 79- 3	8U24	ECL
U 79- 4	P4F6	ECL
U 79- 5	PPHP	ECL
U 79- 6	4CC2	ECL
U 79- 7	PFH9	ECL
U 79- 9	U5C3	ECL
U 79-10	PFH9	ECL
U 79-11	U5C3	ECL
U 79-12	low	ECL
U 79-13	080P	ECL
U 80- 2	P4F6	ECL
U 80- 3	P4F6	ECL
U 80- 4	P4F6	ECL
U 80- 5	5HA1	ECL
U 80- 6	P4F6	ECL
U 80- 7	4CC2	ECL
U 80-10	P4F6	ECL
U 80-11	4CC2	ECL
U 80-12	4CC2	ECL
U 80-13	5HA1	ECL

Board # 64621-66503

Test 1: Loop A - VH = 8U24

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 80-14	P24A	ECL
U 80-15	4CC2	ECL
U 81- 4	P4F6	ECL
U 81- 5	PPHP	ECL
U 81- 6	high	ECL
U 81- 7	42C2	ECL
U 81- 9	1C85	ECL
U 81-10	42C2	ECL
U 81-11	1C85	ECL
U 81-12	low	ECL
U 81-13	080P	ECL
U 82- 4	4CC2	ECL
U 82- 5	PPHP	ECL
U 82- 6	5HA1	ECL
U 82- 7	PFH9	ECL
U 82- 9	U5C3	ECL
U 82-10	PFH9	ECL
U 82-11	U5C3	ECL
U 82-12	low	ECL
U 82-13	080P	ECL
U 85- 5	AHP0	
U 85-10	872A	
U 85-11	6110	
U 85- 4	22F4	ECL
U 85-12	080P	ECL
U 85-13	PP34	ECL
U 89- 1	high	
U 96-11	7755	
U 96-12	U871	
U 96-13	high	

U 99-11	7755
U 99-12	8U24
TOTLZ =	70347
U 99-13	U871
U100- 1	1UPP
U100- 2	C4F8
U100- 3	A192
U100- 4	8877
U100- 5	7755
U100- 7	8877
U100- 9	high
U100-10	high
U100-11	high
U100-12	high
U101- 1	1UPP
U101- 2	C4F8
U101- 3	A192
U101- 4	0753
U101- 5	U871
U101- 6	1407
U101- 7	AHP0
U101- 9	6110
U101-10	872A
U101-11	FFU9
U101-12	9U0H
U101-13	25HU
U101-14	5A59
U101-15	73AU
U102- 1	1UPP
U102- 2	C4F8
U102- 3	A192
U102- 4	0753
U102- 5	U871
U102- 6	9C23
U102- 7	7H09
U102- 9	high
U102-10	6C7U

U102-11	8U24
U102-12	high
U102-13	high
U102-14	9153
U102-15	2FF1
U103- 2	8U24
TOTLZ =	0FL0
U103- 3	8U24
U103- 4	6C7U
U103- 6	high
U103- 7	low
U106- 2	8877
U106- 3	8U24
TOTLZ =	0FL0
U106- 4	8U24
TOTLZ =	4641
U106- 5	8U24
TOTLZ =	0LF0
U106- 6	8877
U106- 7	0753
U115- 8	U871
U115- 9	7755
U115-12	1407
U115-13	9C23
U117- 2	0000
TOTLZ =	1
U117- 3	7H09
U117-13	$$$$
U118- 2	8U24
U118- 3	8U24
TOTLZ =	0FL0
U118-11	0000
TOTLZ =	70347

Board # 64621-66503

Test 1: Loop A - VH = 8U24

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U119- 2	1UPP	U120-18	508P	U122-11	high
U119- 3	1UPP	U120-19	low	U122-12	357P
U119- 4	C4F8			U122-13	high
U119- 5	C4F8			U122-14	99F7
U119- 6	A192	U121- 1	7755	U122-15	low
U119- 7	A192	U121- 2	508P	U122-16	6302
U119- 8	9C23	U121- 3	6302	U122-17	high
U119- 9	9C23	U121- 4	99F7	U122-18	508P
U119-11	0000	U121- 5	357P	U122-19	8877
U119-12	8877	U121- 6	A59P		
U119-13	8877	U121- 7	4871		
U119-14	8U24	U121- 8	8PC9	U123- 1	high
TOTLZ =	0FL0	U121- 9	048C	U123- 2	low
U119-15	8U24	U121-11	048C	U123- 3	high
U119-16	U871	U121-12	8PC9	U123- 4	5401
U119-17	U871	U121-13	4871	U123- 5	57U4
U119-18	high	U121-14	A59P	U123- 6	low
U119-19	high	U121-15	357P	U123- 7	high
		U121-16	99F7	U123- 9	high
		U121-17	6302	U123-11	high
U120- 2	high	U121-18	508P	U123-12	C3HA
U120- 3	048C	U121-19	0000	U123-13	9361
U120- 4	8PC9			U123-14	high
U120- 5	low				
U120- 6	low	U122- 1	8877		
U120- 7	4871	U122- 2	high	U125- 4	0000
U120- 8	A59P	U122- 3	048C		
U120-11	high	U122- 4	high		
U120-13	357P	U122- 5	8PC9	U127- 4	0000
U120-14	99F7	U122- 6	low	TOTLZ =	70347
U120-16	high	U122- 7	4871	U127- 5	U871
U120-17	6302	U122- 8	$$$$	U127- 6	U871
		U122- 9	A59P		

Board # 64621-66503 **Test 2: Loop B - VH = 0418**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 1-17	99CA	U102-10	PP46	U121- 1	AH41
U 1-18	A22H	U102-12	F513	U121- 2	3831
U 1-19	F513			U121- 4	ACHH
U 1-20	3831			U121-16	ACHH
		U103- 2	2H4F	U121-18	3831
		U103- 3	2H4F	U121-19	0000
U102- 1	820F	U103- 4	PP46		
U102- 2	PP46	U103- 7	A22H		
U102- 3	F513			U122- 1	AH41
U102- 4	A959			U122- 6	99CA
U102- 5	A959	U118- 2	2H4F	U122-14	ACHH
U102- 6	0418	U118- 3	2H4F		
TOTLZ = 6027		U118-11	0000		
		TOTLZ = 982			

Model 64621A - Performance Verification

Board # 64621-66503 | Test 3: Loop C - VH = C811

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 25-13	993U	
U 25-14	6H99	
U 25-15	92PC	
U 25-16	0F97	
U 25-26	0F97	
U 25-28	A384	
U 25- 9	high	ECL
U 52- 5	C851	
U 52-10	C80P	
U 52- 2	C851	ECL
U 52- 4	C80P	ECL
U 52-12	C851	ECL
U 52-15	C80P	ECL
U102- 1	09H2	
U102- 2	0A7F	
U102- 3	6HH9	
U102- 4	CC76	
U102- 5	CC76	
U102- 6	C851	
U102-13	6H99	
U121- 1	0367	
U121- 2	993U	
U121- 3	92PC	
U121- 8	6HH9	
U121- 9	1861	
U121-11	1861	
U121-12	6HH9	
U121-17	92PC	
U121-18	993U	
U121-19	0000	

TOTLZ = 213

U122- 1	0367
U122- 3	1861
U122- 5	6HH9
U122-15	A384
U122-17	0F97

Board # 64621-66503

Test 4: Loop D - VH = AU30

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 1-18 CAUH
U 1-19 0U6H
U 1-20 6297
U 1-34 2277
U 1-35 AU30
TOTLZ = 283

U 1- 1 U613 ECL
U 1- 2 492F ECL
U 1- 3 0000 ECL
TOTLZ = 67701
U 1- 4 7UC4 ECL
U 1- 5 80C7 ECL
U 1- 6 FH4A ECL
U 1- 7 AU88 ECL
U 1- 8 14CU ECL
U 1- 9 H026 ECL
U 1-10 1164 ECL
U 1-11 126C ECL
U 1-12 H026 ECL
U 1-16 0000 ECL
TOTLZ = 67701
U 1-21 7F2F ECL
U 1-30 3U78 ECL
U 1-33 0000 ECL
TOTLZ = 67701
U 1-36 FP73 ECL
U 1-37 PA12 ECL
U 1-38 2020 ECL
U 1-39 69P1 ECL
U 1-40 3U78 ECL

U 5- 2 0000 ECL
TOTLZ = 66382
U 5- 3 0000 ECL
TOTLZ = 66382
U 5- 4 0000 ECL
U 5- 5 H026 ECL
U 5- 6 0000 ECL
U 5- 7 H026 ECL
U 5-10 0000 ECL
U 5-11 7UC4 ECL
U 5-14 0000 ECL
TOTLZ = 531

U 6-11 low ECL
U 6-14 high ECL

U 16- 2 492F ECL
U 16- 3 F6UC ECL
U 16- 5 low ECL
U 16- 6 A60A ECL
U 16- 7 UH44 ECL

U 17- 2 94FH ECL
U 17- 3 741A ECL
U 17- 4 8505 ECL
U 17- 5 15FH ECL
U 17- 6 CAUH ECL
U 17- 7 low ECL
U 17- 9 low ECL
U 17-10 high ECL
U 17-11 F6UC ECL
U 17-12 7CC8 ECL
U 17-13 5451 ECL
U 17-14 0837 ECL
U 17-15 4F4F ECL

U 18- 2 H772 ECL
U 18- 3 3500 ECL
U 18- 4 AU30 ECL
TOTLZ = 0
U 18- 5 15FH ECL
U 18- 6 8505 ECL
U 18- 7 PC61 ECL
U 18- 9 7F78 ECL
U 18-10 A2UF ECL
U 18-11 H31H ECL
U 18-12 7CC8 ECL
U 18-13 5451 ECL
U 18-14 7933 ECL
U 18-15 FF08 ECL

U 19- 9 8505 ECL
U 19-12 CAUH ECL
U 19-15 69P1 ECL

U 20- 3 PCCF ECL
U 20- 6 448F ECL
U 20- 7 0000 ECL
TOTLZ = 67701

U 36- 2 3U78 ECL
U 36- 4 AU88 ECL
U 36- 6 5U93 ECL
U 36- 7 70CH ECL
U 36- 8 PF6C ECL
U 36- 9 H772 ECL
U 36-10 FF08 ECL
U 36-11 7933 ECL
U 36-13 741A ECL
U 36-14 94FH ECL
U 36-15 4F4F ECL
U 36-16 0837 ECL
U 36-17 3500 ECL
U 36-18 6U93 ECL
U 36-19 8401 ECL
U 36-21 492F ECL
U 36-23 high ECL

U 38- 2 2020 ECL
U 38- 4 FP73 ECL
U 38- 6 6297 ECL
U 38- 7 H410 ECL
U 38- 8 PF6C ECL
U 38- 9 H772 ECL
U 38-10 FF08 ECL
U 38-11 7933 ECL
U 38-13 741A ECL
U 38-14 94FH ECL
U 38-15 4F4F ECL
U 38-16 0837 ECL
U 38-17 3500 ECL
U 38-18 FP49 ECL
U 38-19 0C9C ECL
U 38-21 PA12 ECL
U 38-23 3U78 ECL

U 40- 2 U15C ECL
U 40- 4 3357 ECL
U 40- 6 5U93 ECL

Board # 64621-66503 **Test 4: Loop D - VH = AU30**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 40- 7	70CH	ECL
U 40- 8	5388	ECL
U 40- 9	H772	ECL
U 40-10	FF08	ECL
U 40-11	7933	ECL
U 40-13	741A	ECL
U 40-14	94FH	ECL
U 40-15	4F4F	ECL
U 40-16	0837	ECL
U 40-17	3500	ECL
U 40-18	6U93	ECL
U 40-19	8401	ECL
U 40-21	4F3F	ECL
U 40-23	3HA7	ECL
U 42- 2	PC61	ECL
U 42- 4	7F78	ECL
U 42- 6	6297	ECL
U 42- 7	H410	ECL
U 42- 8	5388	ECL
U 42- 9	H772	ECL
U 42-10	FF08	ECL
U 42-11	7933	ECL
U 42-13	741A	ECL
U 42-14	94FH	ECL
U 42-15	4F4F	ECL
U 42-16	0837	ECL
U 42-17	3500	ECL
U 42-18	FP49	ECL
U 42-19	0C9C	ECL
U 42-21	A2UF	ECL
U 42-23	H31H	ECL
U 43- 3	PCCF	ECL
U 43- 5	0000	ECL
TOTLZ = 67701		
U 43- 6	0000	ECL
TOTLZ = 67701		
U 43- 7	448F	ECL
U 52- 7	15FH	
U 52- 1	15FH	ECL
U 52- 3	CAUH	ECL

U 58- 1	88U0	ECL
U 58- 2	7038	ECL
U 58- 3	low	ECL
U 58- 4	70CH	ECL
U 58- 5	5U93	ECL
U 58- 6	H31H	ECL
U 58- 7	A2UF	ECL
U 58- 9	7F78	ECL
U 58-10	PC61	ECL
U 58-11	6U93	ECL
U 58-12	8401	ECL
U 58-13	58C9	ECL
U 58-14	H7U0	ECL
U 58-15	6261	ECL
U 59- 1	FC55	ECL
U 59- 2	4685	ECL
U 59- 3	low	ECL
U 59- 4	70CH	ECL
U 59- 5	5U93	ECL
U 59- 6	H31H	ECL
U 59- 7	A2UF	ECL
U 59- 9	7F78	ECL
U 59-10	PC61	ECL
U 59-11	6U93	ECL
U 59-12	8401	ECL
U 59-13	4022	ECL
U 59-14	82P0	ECL
U 59-15	FP66	ECL
U 60- 1	A2H9	ECL
U 60- 2	HP6A	ECL
U 60- 3	low	ECL
U 60- 4	H410	ECL
U 60- 5	6297	ECL
U 60- 6	H31H	ECL
U 60- 7	A2UF	ECL
U 60- 9	7F78	ECL
U 60-10	PC61	ECL
U 60-11	FP49	ECL
U 60-12	0C9C	ECL
U 60-13	58C9	ECL
U 60-14	2708	ECL
U 60-15	F7P6	ECL

U 61- 1	19UP	ECL
U 61- 2	8CCC	ECL
U 61- 3	low	ECL
U 61- 4	H410	ECL
U 61- 5	6297	ECL
U 61- 6	H31H	ECL
U 61- 7	A2UF	ECL
U 61- 9	7F78	ECL
U 61-10	PC61	ECL
U 61-11	FP49	ECL
U 61-12	0C9C	ECL
U 61-13	4022	ECL
U 61-14	2A78	ECL
U 61-15	113C	ECL
U 62- 5	5388	
U 62- 7	PF6C	
U 62-10	58C9	
U 62-11	4022	
U 62- 1	PF6C	ECL
U 62- 2	5388	ECL
U 62-14	4022	ECL
U 62-15	58C9	ECL
U 63- 5	6297	
U 63- 7	H410	
U 63-10	0C9C	
U 63-11	FP49	
U 63- 1	H410	ECL
U 63- 2	6297	ECL
U 63-14	FP49	ECL
U 63-15	0C9C	ECL
U 64- 5	5U93	
U 64- 7	70CH	
U 64-10	8401	
U 64-11	6U93	
U 64- 1	70CH	ECL
U 64- 2	5U93	ECL
U 64-14	6U93	ECL
U 64-15	8401	ECL

Board # 64621-66503

Test 4: Loop D - VH = AU30

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

```
U 65- 5  PCCF
U 65- 6  448F  ECL
U 65- 7  PCCF  ECL

U 66- 4  PCCF
U 66- 5  PCCF
U 66-12  AU30

U 68- 1  CA14
U 68- 2  8401
U 68- 3  33C6
U 68- 4  0HP6
U 68- 5  6U93
U 68- 6  70CH
U 68- 7  FC20
U 68- 8  65U9
U 68- 9  5U93
U 68-11  PCCF
U 68-12  0C9C
U 68-13  19PU
U 68-14  83H3
U 68-15  FP49
U 68-16  H410
U 68-17  0C71
U 68-18  07H0
U 68-19  6297

U 78- 4  A60A  ECL
U 78- 5  U15C  ECL
U 78- 6  0F48  ECL
U 78- 7  7038  ECL
U 78- 9  88U0  ECL
U 78-10  6261  ECL
U 78-11  H7U0  ECL
U 78-13  1628  ECL

U 79- 4  8390  ECL
U 79- 5  U15C  ECL
U 79- 6  0H42  ECL
U 79- 7  4685  ECL
U 79- 9  FC55  ECL
U 79-10  FP66  ECL
U 79-11  82P0  ECL
U 79-13  1628  ECL

U 80- 2  0F48  ECL
U 80- 3  UH44  ECL
U 80- 4  UH44  ECL
U 80- 5  3357  ECL
U 80- 6  8390  ECL
U 80- 7  4F98  ECL
U 80- 9  AU30  ECL
TOTLZ = 0
U 80-10  8390  ECL
U 80-11  0H42  ECL
U 80-12  4F98  ECL
U 80-13  3357  ECL
U 80-14  U46F  ECL
U 80-15  0H42  ECL

U 81- 4  UH44  ECL
U 81- 5  U15C  ECL
U 81- 6  U46F  ECL
U 81- 7  HP6A  ECL
U 81- 9  A2H9  ECL
U 81-10  F7P6  ECL
U 81-11  2708  ECL
U 81-13  1628  ECL

U 82- 4  4F98  ECL
U 82- 5  U15C  ECL
U 82- 6  3357  ECL
U 82- 7  8CCC  ECL
U 82- 9  19UP  ECL
U 82-10  113C  ECL
U 82-11  2A78  ECL
U 82-13  1628  ECL

U 83- 4  741A
U 83- 5  94FH
U 83-12  4F4F
U 83-13  0837

U 83- 3  741A  ECL
U 83- 7  94FH  ECL
U 83-11  4F4F  ECL
U 83-15  0837  ECL

U 84- 4  3500
U 84- 5  H772
U 84-12  FF08
U 84-13  7933

U 84- 3  3500  ECL
U 84- 7  H772  ECL
U 84-11  FF08  ECL
U 84-15  7933  ECL

U 85- 5  H488
U 85- 7  448F
U 85-10  C918
U 85-11  UC61

U 85- 1  448F  ECL
U 85- 4  7CC8  ECL
U 85-12  1628  ECL
U 85-13  5451  ECL

U 89- 1  1852
U 89- 2  8401
U 89- 3  7933
U 89- 4  FF08
U 89- 5  6U93
U 89- 6  70CH
U 89- 7  H772
U 89- 8  3500
U 89- 9  5U93
U 89-11  PCCF
U 89-12  0C9C
U 89-13  0837
U 89-14  4F4F
U 89-15  FP49
U 89-16  H410
U 89-17  94FH
U 89-18  741A
U 89-19  6297

U 98- 1  29H4
U 98- 5  AU30
TOTLZ = 583
U 98- 7  C6U5
```

Board # 64621-66503 **Test 4: Loop D - VH = AU30**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 98-10	2277
U 98-12	9339
U 98-13	664F
U 98-14	664F
U100- 1	PAC5
U100- 2	9147
U100- 3	F89F
U100- 4	87P4
U100- 5	87P4
U100- 7	25A2
U100- 9	1852
U100-10	high
U100-11	high
U100-12	CA14
U101- 1	PAC5
U101- 2	9147
U101- 3	F89F
U101- 4	6F58
U101- 5	28H4
U101- 6	73A3
U101- 7	H488
U101- 9	UC61
U101-10	C918
U101-11	5388
U101-12	FF6C
U101-13	4022
U101-14	58C9
U101-15	422A
U102- 1	PAC5
U102- 2	9147
U102- 3	F89F
U102- 4	6F58
U102- 5	28H4
U102- 6	HF93
U102- 7	29H4
U102- 9	9339
U104- 1	29H4
U104- 2	AU30
TOTLZ = 531	
U104-11	19PU
U104-12	83H3
U104-13	0C71
U104-14	07H0
U104-15	P17F
U105- 1	29H4
U105- 2	AU30
U105-10	P17F
U105-11	33C6
U105-12	0HP6
U105-13	FC20
U105-14	65U9
U105-15	F0H5
U106- 2	F368
U106- 3	PCCF
U106- 4	PCCF
U118- 2	664F
U118- 3	664F
U118-11	0000
TOTLZ = 98693	
U121- 1	87P4
U121- 2	6291
U121- 3	H410
U121- 4	FP49
U121- 5	0C9C
U121- 6	5U93
U121- 7	70CH
U121- 8	6U93
U121- 9	8401
U121-11	8401
U121-12	6U93
U121-13	70CH
U121-14	5U93
U121-15	0C9C
U121-16	FP49
U121-17	H410
U121-18	6297
U121-19	0000
U122- 1	25A2
U122- 4	C6U5
U122-16	H410
U125- 1	448F
U125- 2	28H4
U125- 3	PCCF
U127- 6	28H4

Board # 64621-66503

Test 5: Loop E - VH = U16U

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

```
U  1-17  C330
U  1-18  low
U  1-19  3113
U  1-20  60FU
U  1-34  3401
U  1-35  high

U  1- 2  low   ECL
U  1- 3  0000  ECL
TOTLZ = 6550
U  1- 4  993H  ECL
U  1- 7  87AF  ECL
U  1- 8  3178  ECL
U  1-16  0000  ECL
TOTLZ = 6550
U  1-21  81F1  ECL
U  1-30  low   ECL
U  1-33  0000  ECL
TOTLZ = 6550
U  1-36  87AF  ECL
U  1-37  9U64  ECL
U  1-38  9U64  ECL
U  1-39  high  ECL
U  1-40  9U64  ECL

U  5-10  0000  ECL
U  5-11  993H  ECL
U  5-12  U16U  ECL
TOTLZ = 6550
U  5-13  U16U  ECL
U  5-14  0000  ECL
TOTLZ = 19
U  5-15  U16U  ECL

U 16- 9  U16U  ECL
U 16-12  0000  ECL
TOTLZ = 6550
U 16-13  0000  ECL
TOTLZ = 6550

U 19- 3  38U9  ECL
U 19- 6  F996  ECL
U 19- 7  F996  ECL

U 20- 2  6852  ECL
U 20- 5  993H  ECL

U 45-12  0000  ECL
TOTLZ = 6550
U 45-13  6852  ECL
U 45-15  0000  ECL
TOTLZ = 6531

U 66- 4  38U9
U 66-13  U16U

U 66- 2  F996  ECL
U 66- 3  38U9  ECL
U 66-14  0000  ECL
U 66-15  U16U  ECL
TOTLZ = 6550

U 69- 1  830A
U 69- 2  0049
U 69- 3  9PAU
U 69- 4  5380
U 69- 5  040P
U 69- 6  3797
U 69- 7  C234
U 69- 8  762C
U 69- 9  P7U2
U 69-11  38U9
U 69-12  00PH
U 69-13  9054
U 69-14  FCCP
U 69-15  717H
U 69-16  3U21
U 69-17  8U36
U 69-18  A483
U 69-19  60FU

U 71- 1  high
U 71- 2  high
U 71- 3  high
U 71- 4  U16U
TOTLZ = 6510
U 71- 5  high
U 71- 6  high
U 71- 7  high
U 71- 9  6536
U 71-10  762C
U 71-11  9U15
U 71-12  C234
U 71-13  6960
U 71-14  5380
U 71-15  POUH
U 71-16  9PAU
U 71-18  9U7P
U 71-20  U16U
TOTLZ = 6510
U 71-21  high

U 72- 1  high
U 72- 2  high
U 72- 3  high
U 72- 4  U16U
U 72- 5  high
U 72- 6  high
U 72- 7  high
U 72- 9  7020
U 72-10  762C
U 72-11  7190
U 72-12  C234
U 72-13  4FAU
U 72-14  5380
U 72-15  CPC6
U 72-16  9PAU
U 72-18  U35F
U 72-20  U16U
TOTLZ = 19
U 72-21  high

U 77- 4  7020
U 77- 5  7190
U 77-12  4FAU
U 77-13  CPC6

U 77- 3  7020  ECL
U 77- 7  7190  ECL
U 77-11  4FAU  ECL
U 77-15  CPC6  ECL
```

Board # 64621-66503 **Test 5: Loop E - VH = U16U**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

```
U 85- 7  F996

U 85- 1  F996  ECL

U 87- 1  U16U
TOTLZ = 6550
U 87- 2  F9PC
U 87- 3  low
U 87- 4  U16U
U 87- 5  5CF3
U 87- 6  low
U 87- 7  high
U 87- 9  high
U 87-10  low
U 87-11  low
U 87-12  high
U 87-13  low
U 87-14  low

U 88- 1  U16U
U 88- 2  low
U 88- 3  low
U 88- 4  high
U 88- 5  low
U 88- 6  low
U 88- 7  high
U 88- 9  high
U 88-10  low
U 88-11  low
U 88-12  high
U 88-13  low
U 88-14  low

U 91- 1  high
U 91- 2  high
U 91- 3  high
U 91- 4  U16U
TOTLZ = 6510
U 91- 5  high
U 91- 6  high
U 91- 7  high
U 91- 9  354P
U 91-10  A483
U 91-11  99U4
U 91-12  8U36
U 91-13  2HP6
U 91-14  FCCP
U 91-15  1H31
U 91-16  9054
U 91-18  9U7P
U 91-20  U16U
TOTLZ = 19
U 91-21  high

U 92- 1  high
U 92- 2  high
U 92- 3  high
U 92- 4  U16U
TOTLZ = 6510
U 92- 5  high
U 92- 6  high
U 92- 7  high
U 92- 9  66P4
U 92-10  A483
U 92-11  U4UP
U 92-12  8U36
U 92-13  1U75
U 92-14  FCCP
U 92-15  16C2
U 92-16  9054
U 92-18  U35F
U 92-20  U16U
TOTLZ = 19
U 92-21  high

U 93- 1  high
U 93- 2  high
U 93- 3  high
U 93- 4  U16U
TOTLZ = 6510
U 93- 5  high
U 93- 6  high
U 93- 7  high
U 93- 9  796A
U 93-10  A483
U 93-11  6872
U 93-12  8U36
U 93-13  028P
U 93-14  FCCP
U 93-15  8173
U 93-16  9054
U 93-18  POU5
U 93-20  U16U
TOTLZ = 19
U 93-21  high

U 94- 4  796A
U 94- 5  6872
U 94-12  028P
U 94-13  8173

U 94- 3  796A  ECL
U 94- 7  6872  ECL
U 94-11  028P  ECL
U 94-15  8173  ECL

U100- 1  67UC
U100- 2  56U3
U100- 3  0C1C
U100- 4  67F1
U100- 5  67F1
U100-10  830A

U102- 1  67UC
U102- 2  56U3
U102- 3  0C1C
U102- 4  5U38
U102- 5  96AP
U102- 6  CH62
U102- 7  U023
U102-11  F37F

U104- 1  U023
U104- 2  U16U
TOTLZ = 19
U104-11  low
U104-12  low
U104-13  5CF3
U104-14  F9PC
U104-15  low
```

Board # 64621-66503

Test 5: Loop E - VH = U16U

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U105- 1 U023
U105- 2 U16U
U105-10 low
U105-11 low
U105-12 low
U105-13 low
U105-14 low

U106- 9 7HC8
U106-10 POU5
U106-11 U35F
U106-12 9U7P
U106-13 9H4H
U106-14 8PP4

U107- 2 6085
U107- 3 6085
U107- 4 F996
U107- 6 8PP4
U107-10 9H4H
U107-12 F996
U107-13 79H2
U107-14 79H2

U108- 4 354P
U108- 5 99U4
U108-12 2HP6
U108-13 1H31

U108- 3 354P ECL
U108- 7 99U4 ECL
U108-11 2HP6 ECL
U108-15 1H31 ECL

U109- 4 6536
U109- 5 9U15
U109-12 6960
U109-13 POUH

U109- 3 6536 ECL
U109- 7 9U15 ECL
U109-11 6960 ECL
U109-15 POUH ECL

U110- 4 66P4
U110- 5 U4UP
U110-12 1U75
U110-13 16C2

U110- 3 66P4 ECL
U110- 7 U4UP ECL
U110-11 1U75 ECL
U110-15 16C2 ECL

U112- 8 low
U112- 9 A14F

U112- 2 CPC6 ECL
U112- 3 796A ECL
U112- 4 6872 ECL
U112- 5 028P ECL
U112- 6 8173 ECL
U112-14 354P ECL
U112-15 99U4 ECL
U112-16 2HP6 ECL
U112-17 1H31 ECL
U112-18 6536 ECL
U112-19 9U15 ECL
U112-20 6960 ECL
U112-21 POUH ECL
U112-22 66P4 ECL
U112-23 U4UP ECL
U112-25 0000 ECL
TOTLZ = 19
U112-26 0000 ECL
TOTLZ = 6550
U112-27 0000 ECL

TOTLZ = 6531
U112-32 81F1 ECL
U112-36 1U75 ECL
U112-37 16C2 ECL
U112-38 7020 ECL
U112-39 7190 ECL
U112-40 4FAU ECL

U120-11 F37F
U120-16 A14F
U120-17 3U21
U120-18 60FU
U120-19 low

U121- 1 67F1
U121- 2 60FU
U121- 3 3U21
U121- 4 717H
U121- 5 00PH
U121- 6 P7U2
U121- 7 3797
U121- 8 040P
U121- 9 0049
U121-11 0049
U121-12 040P
U121-13 3797
U121-14 P7U2
U121-15 00PH
U121-16 717H
U121-17 3U21
U121-18 60FU
U121-19 0000
TOTLZ = 34488

U125- 1 F996
U125- 2 96AP
U125- 3 38U9

Board # 64621-66503 Test 6: Loop F - VH = 894H; QUAL - VH = PFA4

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
QUAL:	Stop - Negative	Clock - TTL	Clock - U99 pin 3
High		ST-SP-QL - TTL	Ground - GND (TP)
------			Qual - U100 pin 7

** = levels are TTL except where noted.

U 1- 4 low
U 1-17 2362
U 1-18 CAHC
U 1-19 6192
U 1-20 FF34
U 1-34 34F8
U 1-35 A336

U 1- 2 3174 ECL
U 1- 3 0000 ECL
TOTLZ = 0LF0
U 1- 4 F23A ECL
U 1- 7 4314 ECL
U 1- 8 FU0C ECL
U 1- 9 HC41 ECL
U 1-12 HC41 ECL
U 1-16 0000 ECL
U 1-21 74P2 ECL
U 1-30 19F2 ECL
U 1-33 0000 ECL
TOTLZ = 0FL0
U 1-36 5AH6 ECL
U 1-37 5AH6 ECL
U 1-38 5AH6 ECL
U 1-39 3396 ECL
U 1-40 5AH6 ECL

U 5- 3 0000 ECL
TOTLZ = 0FL0
U 5- 6 0000 ECL
U 5- 7 HC41 ECL
U 5-10 0000 ECL
U 5-11 F23A ECL
U 5-12 894H ECL
TOTLZ = 0FL0
U 5-13 894H ECL
U 5-14 0000 ECL
TOTLZ = 0FL0
U 5-15 894H ECL

U 16- 9 894H ECL
U 16-12 0000 ECL
TOTLZ = 0FL0
U 16-13 0000 ECL
TOTLZ = 0FL0

U 19- 2 FF68 ECL
U 19- 3 4525 ECL
U 19- 4 4525 ECL
U 19- 5 4525 ECL
U 19- 6 FF68 ECL
U 19- 7 FF68 ECL

U 20- 2 4C77 ECL
U 20- 5 F23A ECL

U 45-12 0000 ECL
U 45-13 4C77 ECL
U 45-15 0000 ECL
TOTLZ = 0FL0

U 65-13 0000
TOTLZ = 0FL0

U 66- 4 4525
U 66- 5 4525
U 66-12 894H
TOTLZ = 1796
U 66-13 894H

U 66- 2 FF68 ECL
U 66- 3 4525 ECL
U 66- 6 FF68 ECL
U 66- 7 4525 ECL
U 66-15 894H ECL
TOTLZ = 0FL0

U 67- 1 416P
U 67- 2 80U7
U 67- 3 4P69
U 67- 4 F989
U 67- 5 1108
U 67- 6 F789
U 67- 7 0UH0
U 67- 8 7233
U 67- 9 8PU8
U 67-11 894H
TOTLZ = 0FL0
U 67-12 1U1A QUAL
U 67-13 H219
U 67-14 91C3
U 67-15 6412
U 67-16 A10C
U 67-17 C0UF
U 67-18 7753
U 67-19 FF34

U 68- 1 190C
U 68- 2 80U7
U 68- 3 4P69
U 68- 4 F989
U 68- 5 1108
U 68- 6 F789
U 68- 7 0UH0
U 68- 8 7233
U 68- 9 8PU8
U 68-11 4525
U 68-12 1U1A QUAL
U 68-13 H219
U 68-14 91C3
U 68-15 6412
U 68-16 A10C
U 68-17 C0UF
U 68-18 7753
U 68-19 FF34

U 69- 1 U274
U 69- 2 80U7
U 69- 3 AC8P
U 69- 4 9520
U 69- 5 1108
U 69- 6 F789
U 69- 7 F82U
U 69- 8 641C
U 69- 9 8PU8
U 69-11 4525
U 69-12 1U1A QUAL
U 69-13 FFFP
U 69-14 U87C

Board # 64621-66503

Test 6: Loop F - VH = 894H; QUAL - VH = PFA4

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
QUAL:	Stop - Negative	Clock - TTL	Clock - U99 pin 3
High		ST-SP-QL - TTL	Ground - GND (TP)
------			Qual - U100 pin 7

** = levels are TTL except where noted.

U 69-15 6412
U 69-16 A10C
U 69-17 PUC6
U 69-18 0F8U
U 69-19 FF34

U 70- 1 8989
U 70- 2 50P9
U 70- 3 93A5
U 70- 4 APF4
U 70- 5 C6H0
U 70- 6 FP41
U 70- 7 6HF0
U 70- 9 AAF2
U 70-10 641C
U 70-11 9501
U 70-12 F82U
U 70-13 3733
U 70-14 9520
U 70-15 P0AU
U 70-16 AC8P
U 70-18 63PH
U 70-20 894H
TOTLZ = 1796
U 70-21 3781

U 71- 1 8989
U 71- 2 50P9
U 71- 3 93A5
U 71- 4 APF4
U 71- 5 C6H0
U 71- 6 FP41
U 71- 7 6HF0
U 71- 9 HU5A
U 71-10 641C
U 71-11 A0C7
U 71-12 F82U
U 71-13 4214
U 71-14 9520
U 71-15 16U4
U 71-16 AC8P
U 71-18 018F
U 71-20 894H
TOTLZ = 1796
U 71-21 3781

U 72- 1 8989
U 72- 2 50P9
U 72- 3 93A5
U 72- 4 APF4
U 72- 5 C6H0
U 72- 6 FP41
U 72- 7 6HF0
U 72- 9 8F6A
U 72-10 641C
U 72-11 1F56
U 72-12 F82U
U 72-13 HU5A
U 72-14 9520
U 72-15 A0C7
U 72-16 AC8P
U 72-18 05C7
U 72-20 894H
TOTLZ = 1796
U 72-21 3781

U 73- 1 8989
U 73- 2 50P9
U 73- 3 93A5
U 73- 4 APF4
U 73- 5 C6H0
U 73- 6 FP41
U 73- 7 6HF0
U 73-10 641C
U 73-11 FU0C
U 73-12 F82U
U 73-13 UHAU
U 73-14 9520
U 73-15 high
U 73-16 AC8P
U 73-18 PP9C
U 73-20 894H
TOTLZ = 1796
U 73-21 3781

U 74- 5 FU0C
U 74-12 UHAU
U 74-13 high

U 74- 7 FU0C ECL
U 74-10 74P2 ECL
U 74-14 low ECL

U 77- 4 8F6A
U 77- 5 1F56
U 77-12 HU5A
U 77-13 A0C7

U 77- 3 8F6A ECL
U 77- 7 1F56 ECL
U 77-11 HU5A ECL
U 77-15 A0C7 ECL

U 83- 4 H9C2
U 83- 5 5AP4
U 83-12 884A
U 83-13 H244

U 84- 4 AAF2
U 84- 5 9501
U 84-12 3733
U 84-13 P0AU

U 85- 7 FF68

U 85- 1 FF68 ECL

U 86- 2 P48H
U 86- 3 8A99
U 86- 4 7920
U 86- 5 470F
U 86- 6 3U9H
U 86- 7 8965
U 86- 8 80H9
U 86- 9 CPFF
U 86-11 FF68
U 86-12 00F4

Board # 64621-66503 Test 6: Loop F - VH = 894H; QUAL - VH = PFA4

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
QUAL:	Stop - Negative	Clock - TTL	Clock - U99 pin 3
High		ST-SP-QL - TTL	Ground - GND (TP)
------			Qual - U100 pin 7

** = levels are TTL except where noted.

U 86-13 P82F
U 86-14 49F1
U 86-15 H9A4
U 86-16 1AP8
U 86-17 4C7F
U 86-18 6F4C
U 86-19 2789

U 87- 1 894H
TOTLZ = 0FL0
U 87- 2 7753
U 87- 3 2789
U 87- 4 APF4
U 87- 5 C0UF
U 87- 6 1AP8
U 87- 7 93A5
U 87- 9 50P9
U 87-10 H9A4
U 87-11 91C3
U 87-12 8989
U 87-13 00F4
U 87-14 H219

U 88- 1 894H
TOTLZ = 0FL0
U 88- 2 7233
U 88- 3 CPFF
U 88- 4 3781
U 88- 5 0UH0
U 88- 6 3U9H
U 88- 7 C6H0
U 88- 9 FP41
U 88-10 470F
U 88-11 F989
U 88-12 6HF0
U 88-13 P48H
U 88-14 4P69

U 90- 1 8989
U 90- 2 50P9
U 90- 3 93A5
U 90- 4 APF4
U 90- 5 C6H0
U 90- 6 FP41
U 90- 7 6HF0
U 90- 9 H9C2
U 90-10 0F8U
U 90-11 5AP4
U 90-12 PUC6
U 90-13 884A
U 90-14 U87C
U 90-15 H244
U 90-16 FFFP
U 90-18 63PH
U 90-20 894H
TOTLZ = 1796
U 90-21 3781

U 91- 1 8989
U 91- 2 50P9
U 91- 3 93A5
U 91- 4 APF4
U 91- 5 C6H0
U 91- 6 FP41
U 91- 7 6HF0
U 91- 9 0A05
U 91-10 0F8U
U 91-11 UAFH
U 91-12 PUC6
U 91-13 8F6A
U 91-14 U87C
U 91-15 1F56
U 91-16 FFFP
U 91-18 018F
U 91-20 894H
TOTLZ = 1796
U 91-21 3781

U 92- 1 8989
U 92- 2 50P9
U 92- 3 93A5
U 92- 4 APF4
U 92- 5 C6H0
U 92- 6 FP41
U 92- 7 6HF0
U 92- 9 U0FP
U 92-10 0F8U
U 92-11 3U98
U 92-12 PUC6
U 92-13 0A05
U 92-14 U87C
U 92-15 UAFH
U 92-16 FFFP
U 92-18 05C7
U 92-20 894H
TOTLZ = 1796
U 92-21 3781

U 93- 1 8989
U 93- 2 50P9
U 93- 3 93A5
U 93- 4 APF4
U 93- 5 C6H0
U 93- 6 FP41
U 93- 7 6HF0
U 93- 9 4214
U 93-10 0F8U
U 93-11 16U4
U 93-12 PUC6
U 93-13 U0FP
U 93-14 U87C
U 93-15 934P
U 93-16 FFFP
U 93-18 PP9C
U 93-20 894H
TOTLZ = 1796
U 93-21 3781

U 94- 4 4214
U 94- 5 16U4
U 94-12 U0FP
U 94-13 934P

U 94- 3 4214 ECL
U 94- 7 16U4 ECL
U 94-11 U0FP ECL
U 94-15 934P ECL

Board # 64621-66503

Test 6: Loop F - VH = 894H; QUAL - VH = PFA4

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
QUAL:	Stop - Negative	Clock - TTL	Clock - U99 pin 3
High		ST-SP-QL - TTL	Ground - GND (TP)
------			Qual - U100 pin 7

** = levels are TTL except where noted.

U 96- 8 894H
TOTLZ = 0FL0
U 96- 9 AF2A
U 96-10 0000
TOTLZ = 0FL0

U 98- 1 5UU6
U 98- 5 A336
U 98- 7 AF2A

U100- 1 80H9
U100- 2 8965
U100- 3 7920
U100- 4 489A
U100- 5 489A
U100- 6 high
U100- 7 6CF6
U100- 9 high
U100-10 U274
U100-11 416P
U100-12 190C

U102- 1 80H9
U102- 2 8965
U102- 3 7920
U102- 4 0HCU
U102- 5 F1H7
U102- 6 8A99
U102- 7 5UU6

U103- 9 HA7A
U103-12 894H
TOTLZ = 1796
U103-14 F6H1
U103-15 5UU6

U104- 1 5UU6
U104- 2 894H
TOTLZ = 1796
U104-11 H219
U104-12 91C3
U104-13 C0UF
U104-14 7753
U104-15 9518

U105- 1 5UU6
U105- 2 894H
U105-10 9518
U105-11 4P69
U105-12 F989
U105-13 0UH0
U105-14 7233
U105-15 F6H1

U106- 9 63PH
U106-10 PP9C
U106-11 05C7
U106-12 018F
U106-13 8H76
U106-14 665A

U107- 2 C6AH
U107- 3 C6AH
U107- 4 FF68
U107- 6 665A
U107-10 8H76
U107-12 FF68
U107-13 CH0P
U107-14 CH0P

U108- 4 0A05
U108- 5 UAFH
U108-12 8F6A
U108-13 1F56

U108- 3 0A05 ECL
U108- 7 UAFH ECL
U108-11 8F6A ECL
U108-15 1F56 ECL

U109- 4 HU5A
U109- 5 A0C7
U109-12 4214
U109-13 16U4

U110- 4 U0FP
U110- 5 3U98
U110-12 0A05
U110-13 UAFH

U110- 3 U0FP ECL
U110- 7 3U98 ECL
U110-11 0A05 ECL
U110-15 UAFH ECL

U112- 8 low
U112- 9 high

U112- 2 A0C7 ECL
U112- 3 4214 ECL
U112- 4 16U4 ECL
U112- 5 U0FP ECL
U112- 6 934P ECL
U112-14 0A05 ECL
U112-15 UAFH ECL
U112-16 8F6A ECL
U112-17 1F56 ECL
U112-18 HU5A ECL
U112-19 A0C7 ECL
U112-20 4214 ECL
U112-21 16U4 ECL
U112-22 U0FP ECL
U112-23 3U98 ECL
U112-25 0000 ECL
TOTLZ = 1796
U112-26 0000 ECL
TOTLZ = 1796
U112-27 0000 ECL
TOTLZ = 1796
U112-32 74P2 ECL
U112-36 0A05 ECL
U112-37 UAFH ECL
U112-38 8F6A ECL
U112-39 1F56 ECL
U112-40 HU5A ECL

U118- 2 C6AH
U118- 3 C6AH
U118- 4 CH0P
U118- 5 CH0P

Board # 64621-66503 **Test 6: Loop F - VH = 894H; QUAL - VH = PFA4**

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
QUAL:	Stop - Negative	Clock - TTL	Clock - U99 pin 3
High		ST-SP-QL - TTL	Ground - GND (TP)
------			Qual - U100 pin 7

** = levels are TTL except where noted.

U118-11 0000	U121-11 80U7	U122- 4 AF2A
TOTLZ = 0FL0	U121-12 1108	U122- 6 2362
	U121-13 F789	U122- 9 8PU8
U121- 1 489A	U121-14 8PU8	U122-11 4525
U121- 2 FF34	U121-15 1U1A QUAL	U122-14 6412
U121- 3 A10C	U121-16 6412	U122-16 A10C
U121- 4 6412	U121-17 A10C	U122-18 FF34
U121- 5 1U1A QUAL	U121-18 FF34	
U121- 6 8PU8	U121-19 0000	U125- 1 FF68
U121- 7 F789	TOTLZ = 0FL0	U125- 2 F1H7
U121- 8 1108		U125- 3 4525
U121- 9 80U7	U122- 1 6CF6	
	U122- 2 HA7A	

Board # 64621-66503

Test 6: Loop G - VH=62A5

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U66 pin 13
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

U 70- 1 87P8
U 70- 2 4040
U 70- 3 7702
U 70- 4 0818
U 70- 5 H473
U 70- 6 8P84
U 70- 7 62H4
U 70- 9 52C6
U 70-11 848U
U 70-13 966C
U 70-15 C49U
U 70-18 564A
U 70-20 736C
U 70-21 995U

U 71- 9 H62P
U 71-11 H23C
U 71-13 1444
U 71-15 A2HC
U 71-18 34PU

U 72- 9 21AC
U 72-11 H173
U 72-13 H62P
U 72-15 H23C
U 72-18 62A5
TOTLZ=768

U 73- 9 low
U 73-11 3254
U 73-12 0C49
U 73-13 61P7
U 73-15 high
U 73-18 62A5
TOTLZ=768

U 87- 1 0000
TOTLZ=0FL0
U 87- 2 6ACH
U 87- 3 62A5
TOTLZ=640
U 87- 4 0818
U 87- 5 15A7
U 87- 6 62A5
TOTLZ=320
U 87- 7 7702
U 87- 9 4040
U 87-10 62A5
TOTLZ=160
U 87-11 22P5
U 87-12 87P8
U 87-13 62A5
TOTLZ=80
U 87-14 P54H

U 88- 1 0000
TOTLZ=0FL0
U 88- 2 UCUA
U 88- 3 62A5
TOTLZ=40
U 88- 4 995U
U 88- 5 C6H6
U 88- 6 62A5
TOTLZ=20
U 88- 7 H473
U 88- 9 8P84
U 88-10 62A5
TOTLZ=10
U 88-11 PF21
U 88-12 62H4
U 88-13 62A5
TOTLZ=5
U 88-14 0071

U 90- 9 030C
U 90-11 H896
U 90-13 HAHA
U 90-15 5HC6
U 90-18 564A

U 91- 9 C830
U 91-11 7391
U 91-13 21AC
U 91-15 H173
U 91-18 34PU

U 92- 9 FA68
U 92-11 2UUA
U 92-13 C830
U 92-14 FH56
U 92-15 7391
U 92-18 62A5
TOTLZ=768

U 93- 1 87P8
U 93- 2 4040
U 93- 3 7702
U 93- 4 0818
U 93- 5 H473
U 93- 6 8P84
U 93- 7 62H4
U 93- 9 1444
U 93-11 A2HC
U 93-13 FA68
U 93-15 FFAH
U 93-18 62A5
TOTLZ=768
U 93-20 736C
U 93-21 995U

Board # 64621-66503

Test 11: Loop H - VH = 7339

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	CLOCK - Positive	Data - High **	ST/SP/Start - TP19
------	START - Positive	Data - Low **	Qual/Stop - TP19
------	STOP - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

NOTE: Remove the clock pod connector from J3.
** = levels are TTL except where noted.

U 1-17 low
U 1-35 high

U 26- 1 00UP
U 26- 2 7338
U 26- 3 7333
U 26- 4 733H
U 26- 5 7331
U 26- 6 7329
U 26- 7 7319
U 26- 8 7379
U 26- 9 73C8
U 26-11 73C8
U 26-12 7379
U 26-13 7319
U 26-14 7329
U 26-15 7331
U 26-16 733H
U 26-17 733C
U 26-18 7338
U 26-19 0000
TOTLZ = 24

U 53- 2 73F7
U 53- 3 8H4A
U 53- 5 659P
U 53- 7 3FU9
U 53- 9 A285
U 53-11 A285
U 53-13 3FU9
U 53-15 659P
U 53-17 8H4A
U 53-18 73F7

U 65- 3 high ECL
U 65- 4 high ECL

U 96- 4 73F7
U 96- 5 00UP
U 96- 6 7339
TOTLZ = 24

U 97- 2 3FU9
U 97- 4 high
U 97- 5 high
U 97- 7 low
U 97- 9 low
U 97-11 low

U 99- 4 low
U 99- 5 high
U 99- 6 high
U 99- 8 high
U 99- 9 low
U 99-10 low

U116- 6 high
U116- 8 low
U116- 9 high

U118- 2 A285
U118- 5 3FU9
U118- 6 659P
U118-11 0000
TOTLZ = 24

U119-16 73F7

U120- 4 733C
U120- 5 low
U120- 6 low
U120- 7 733H
U120-11 high

U123- 1 high
U123- 2 low
U123- 3 high
U123- 6 low
U123- 7 high
U123- 9 high

U127- 1 0000
TOTLZ = 24
U127- 2 0000
TOTLZ = 26
U127- 3 0000
TOTLZ = 24
U127- 8 0000
TOTLZ = 24
U127- 9 0000
TOTLZ = 24

U129- 1 high ECL
U129- 2 0000 ECL
TOTLZ = 24
U129- 3 low ECL
U129- 4 7339 ECL
TOTLZ = 24
U129- 5 high ECL
U129- 6 high ECL
U129-13 low ECL
U129-14 high ECL

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Test 12: Loop I - VH = 9524

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - TP19
------	Start - Positive	Data - Low **	Qual/Stop - TP19
------	Stop - Negative	Clock - TTL	Clock - U99 pin 3
------		ST-SP-QL - TTL	Ground - GND (TP)

** = levels are TTL except where noted.

```
U  1- 3  9524   ECL        U 97-11  8741         U123- 3  high
U  1- 4  high   ECL        U 97-12  F8C7         U123- 4  AFFP
U  1-17  8741              U 97-14  0505         U123- 5  HC26
U  1-35  9524                                    U123- 6  C6F4
TOTLZ = 400                U116- 1  9524         U123- 7  23P0
                           TOTLZ = 400           U123- 9  HH12
U 97- 2  0505              U116- 6  9524         U123-11  C6F4
U 97- 4  F8C7              TOTLZ = 200           U123-12  126F
U 97- 5  9524              U116- 8  0000         U123-13  64P2
TOTLZ = 400                TOTLZ = 400           U123-14  C6F4
U 97- 7  0000              U116- 9  high
TOTLZ = 200                                      U126- 5  52F8
U 97- 9  0000              U123- 1  high         U126- 7  F7PF
TOTLZ = 1                  U123- 2  low          U126-11  F7PF
```

NOTES

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. The Strobe Generator Adjustment procedure is Test 9 of the Performance Verification, and the Threshold Adjustments procedure is Test 10.

5-4. SAFETY REQUIREMENTS.

5-5. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death or damage to equipment. Service adjustments should be performed only by qualified service personnel.

5-6. EQUIPMENT REQUIRED.

5-7. TEST EQUIPMENT.

1. 4 1/2 Digit Multimeter accurate to +/-1 mV. (Hewlett-Packard Model 3466A or equivalent.)

2. Dual Channel 100 MHz bandwidth Oscilloscope with delta time measurement capabilities accurate to 0.5 ns. (Hewlett-Packard Model 1743A with probes.)

5-8. ACCESSORIES.

1. Hewlett-Packard Model 64000 series Mainframe with extender board and SEB Extender Cable.

5-9. PROCEDURE.

5-10. This procedure assumes that all other modules of this system are working properly, and are calibrated and meet or exceed their respective specifications.

NOTE

> Installation and removal of P.C. Boards must be done with the AC Power for the Mainframe turned off.

5-11. STROBE GENERATOR ADJUSTMENTS. (TEST 9)

a. Place the State Analysis Control Board on an extender board. The SEB Bus Cable must be connected to the Acquisition Boards. Use the extreme ends of the cable to avoid reflections.

b. Select opt_test , press RETURN . The display will indicate the option modules present and the card slot number in which they are located.

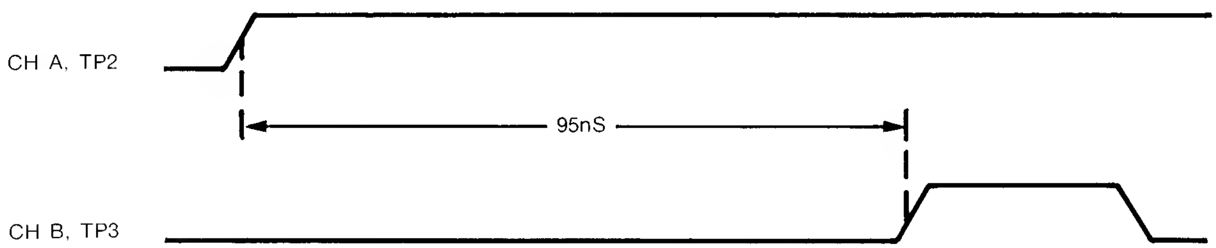
c. Press "slot number" , RETURN . "Slot number" is a number from 0 to 9 equal to the location of the State Analysis Control Board.

d. Press run , "slot number" , test , 9 , repeat , RETURN . The CRT should now display "Test 9: Strobe Generator Calibration".

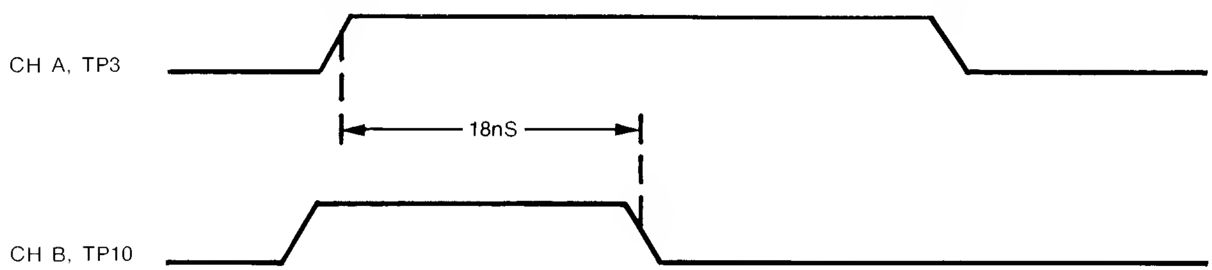
NOTE

All of the following Strobe Generator measurements must be made within +/-0.5 ns of the indicated value. All transitions are measured at the 50% level (ECL Level).

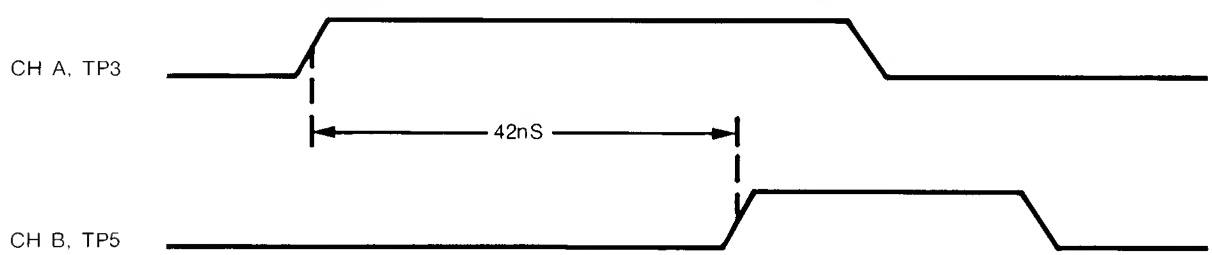
e. Connect channel A of the scope to TP2 (State Recognition Strobe), and trigger on channel A. Connect channel B to TP3 (Pipeline Strobe). Using adjustment T1, (R8), adjust the rising edge of channel B as indicated in the following diagram:



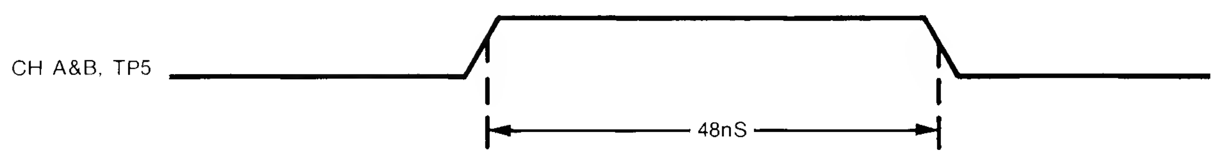
f. Connect channel A to TP3 (Pipeline Strobe), and trigger on channel A. Connect channel B to TP10 (Overview Strobe). Using adjustment T2 (R7), adjust the falling edge of channel B as indicated in the following diagram:



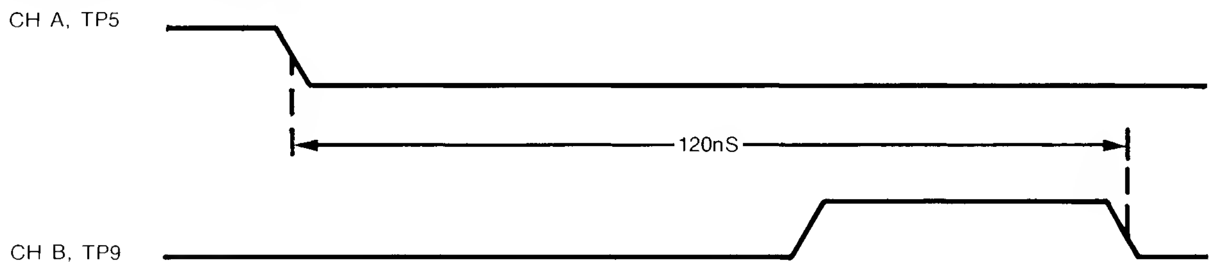
g. Connect channel B to TP5 (Qualified Write Strobe). Channel A remains on TP3, and is the trigger for the scope. Using adjustment T3, (R6), adjust the rising edge of channel B as indicated in the following diagram:



h. Connect channel A and B to TP5 (Qualified Write Strobe). Trigger on channel A. Using adjustment T4, (R5), adjust the pulse width as indicated in the following diagram:



i. Connect channel B to TP9 (data Valid Strobe). Channel A remains on TP5, and is also the trigger. Using adjustment T5 (R4), adjust the falling edge of channel B as indicated in the following diagram:



j. Pressing stop , end , RETURN , end will end the Strobe Generator Calibration Performance Verification.

k. This completes the Strobe Generator Calibration.

5-12. THRESHOLD ADJUSTMENTS. (TEST 10)

a. Place the State Analysis Control Board on an extender board. The IMB and SEB Bus Cables do not need to be connected.

b. If it is not already disconnected, disconnect the Clock Probe Cable from J3.

c. Connect the ground lead of the DMM to the GND TP near U70. See Figure 5-1.

d. Using a jumper wire, connect TP11 and TP12 together.

e. Connect the positive lead of the DMM to Testpoint 11.

f. Select opt_test , press RETURN . The display will indicate the option modules present and the card slot number they are located in.

g. Press "slot number", RETURN . "Slot number" is a number from 1 to 9 equal to the location of the State Analysis Control Board.

h. Press run , "slot number" , test , 1 , 0 , RETURN . The CRT should now display "Test 10:Threshold Circuit Calibration".

i. Each time the RETURN key is pressed, the D/A Converter will be set to a new value. Press RETURN until "Reference = -4.267 V Negative Limit" is displayed.

j. Adjust -FS, R24, to -4.267 V +/- 1 mV. See Figure 5-1.

k. Remove the jumper from TP11 and TP12. Positive lead of the DMM remains on TP11.

l. Continue pressing RETURN until "Reference = +433 mV ECL (-1.3 V)" is displayed.

m. Adjust +FS2, R25, to +433 mV. See Figure 5-1.

n. Each time RETURN is pressed, the D/A Converter will be set to a different value. Press RETURN six times and verify that the value measured on the DMM is within +/-33 mV of the value displayed for all six DAC levels.(If the voltages are not correct, there is most likely a problem in the DAC and must be corrected using the Performance Verification.)

o. Connect the positive lead of the DMM to TP12.

p. Continue pressing RETURN until "Reference = +433 mV ECL (-1.3 V)" is displayed.

q. Adjust +FS1, R23, to +433 mV. See Figure 5-1.

r. Each time RETURN is pressed, the D/A Converter will be set to a different value. Press RETURN six times and verify that the value measured on the DMM is within +/-33 mV of the value displayed for all six DAC levels.(If the voltages are not correct, there is most likely a problem in the DAC and must be corrected using the Performance Verification.)

s. Press end, RETURN, end to exit the State Analysis Control Performance Verification.

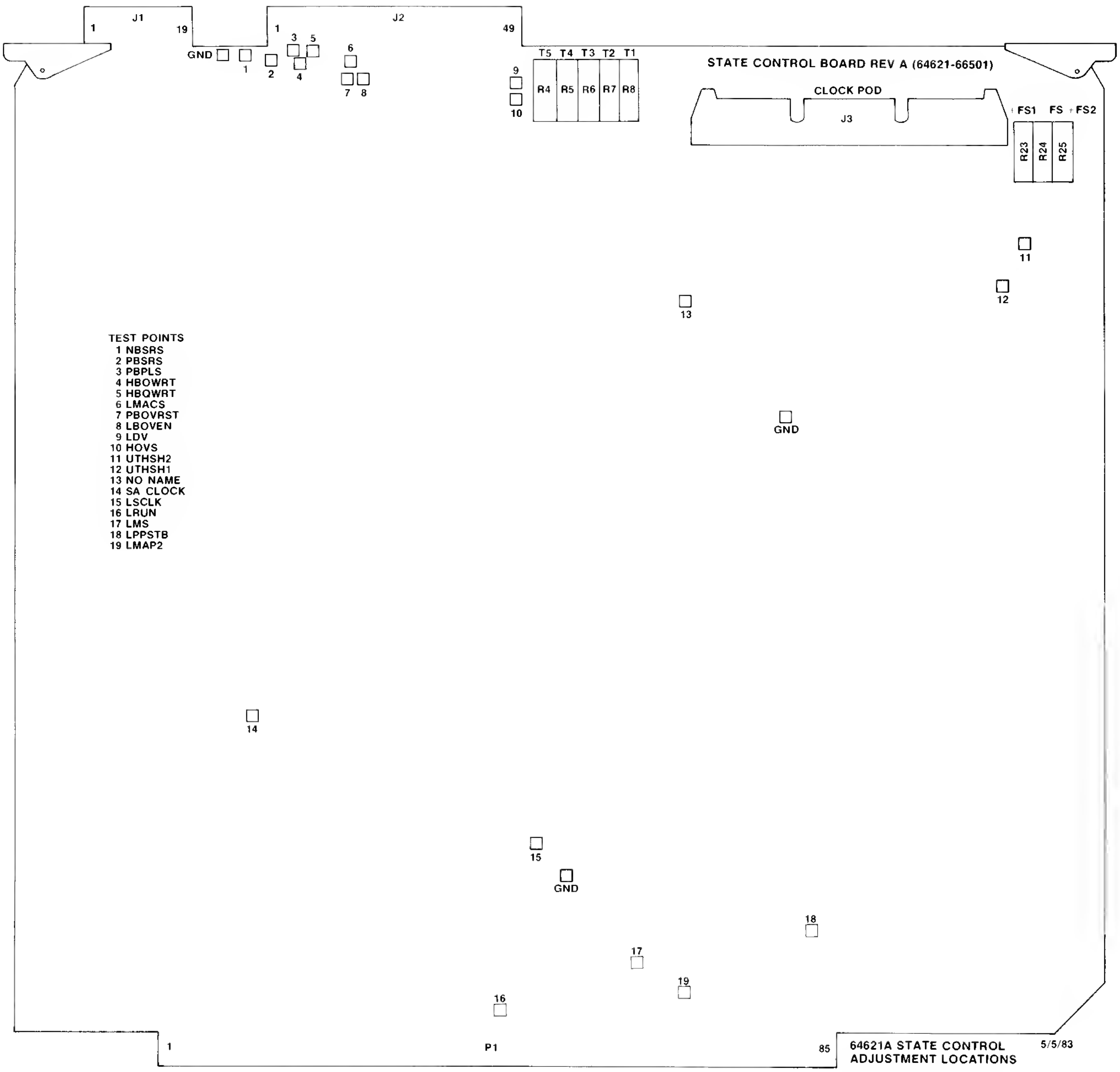


Figure 5-1. Adjustment Locations

NOTES

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturers' part number.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of

the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. SPARE PARTS KIT.

6-11. A spare parts kit is not available at this time.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No Maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices -to provide these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	F	= fuse	MP	= mechanical part	U	= integrated circuit
B	= motor	FL	= filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	IC	= integrated circuit	Q	= transistor		
C	= capacitor	J	= jack	R	= resistor	VR	= voltage regulator
CP	= coupler	K	= relay	RT	= thermistor	W	= cable
CR	= diode	L	= inductor	S	= switch	X	= socket
DL	= delay line	LS	= loud speaker	T	= transformer	Y	= crystal
DS	= device signaling (lamp)	M	= meter	TB	= terminal board	Z	= tuned cavity network
E	= misc electronic part	MK	= microphone	TP	= test point		

ABBREVIATIONS

A	= amperes	H	= henries	N/O	= normally open	RMO	= rack mount only
AFC	= automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	= root-mean square
AMPL	= amplifier	HEX	= hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
BFO	= beat frequency oscillator	HG	= mercury	NPN	= negative-positive-negative	S-B	= slow-blow
BE CU	= beryllium copper	HR	= hour(s)	NRFR	= not recommended for field replacement	SCR	= screw
BH	= binder head	HZ	= hertz	NSR	= not separately replaceable	SE	= selenium
BP	= bandpass	IF	= intermediate freq	OBD	= order by description	SECT	= section(s)
BRS	= brass	IMPG	= impregnated	OH	= oval head	SEMICON	= semiconductor
BWO	= backward wave oscillator	INCD	= incandescent	OX	= oxide	SI	= silicon
CCW	= counter-clockwise	INCL	= include(s)	P	= peak	SIL	= silver
CER	= ceramic	INS	= insulation(ed)	PC	= printed circuit	SL	= slide
CMO	= cabinet mount only	INT	= internal	PF	= picofarads = 10^{-12} farads	SPG	= spring
COEF	= coeficient	K	= kilo = 1000	PH BRZ	= phosphor bronze	SPL	= special
COM	= common	LH	= left hand	PHL	= phillips	SST	= stainless steel
COMP	= composition	LIN	= linear taper	PIV	= peak inverse voltage	SR	= split ring
COMPL	= complete	LK WASH	= lock washer	PNP	= positive-negative-positive	STL	= steel
CONN	= connector	LOG	= logarithmic taper	P/O	= part of	TA	= tantalum
CP	= cadmium plate	LPF	= low pass filter	POLY	= polystyrene	TD	= time delay
CRT	= cathode-ray tube	M	= milli = 10^{-3}	PORC	= porcelain	TGL	= toggle
CW	= clockwise	MEG	= meg = 10^{6}	POS	= position(s)	THD	= thread
DEPC	= deposited carbon	MET FLM	= metal film	POT	= potentiometer	TI	= titanium
DR	= drive	MET OX	= metallic oxide	PP	= peak-to-peak	TOL	= tolerance
ELECT	= electrolytic	MFR	= manufacturer	PT	= point	TRIM	= trimmer
ENCAP	= encapsulated	MHZ	= mega hertz	PWV	= peak working voltage	TWT	= traveling wave tube
EXT	= external	MINAT	= miniature	RECT	= rectifier	U	= micro = 10^{-6}
F	= farads	MOM	= momentary	RF	= radio frequency	VAR	= variable
FH	= flat head	MOS	= metal oxide substrate	RH	= round head or right hand	VDCW	= dc working volts
FIL H	= fillister head	MTG	= mounting			W/	= with
FXD	= fixed	MY	= "mylar"			W	= watts
G	= giga (10^{9})	N	= nano (10^{-9})			WIV	= working inverse voltage
GE	= germanium	N/C	= normally closed			WW	= wirewound
GL	= glass	NE	= neon			W/O	= without
GRD	= ground(ed)	NI PL	= nickel plate				

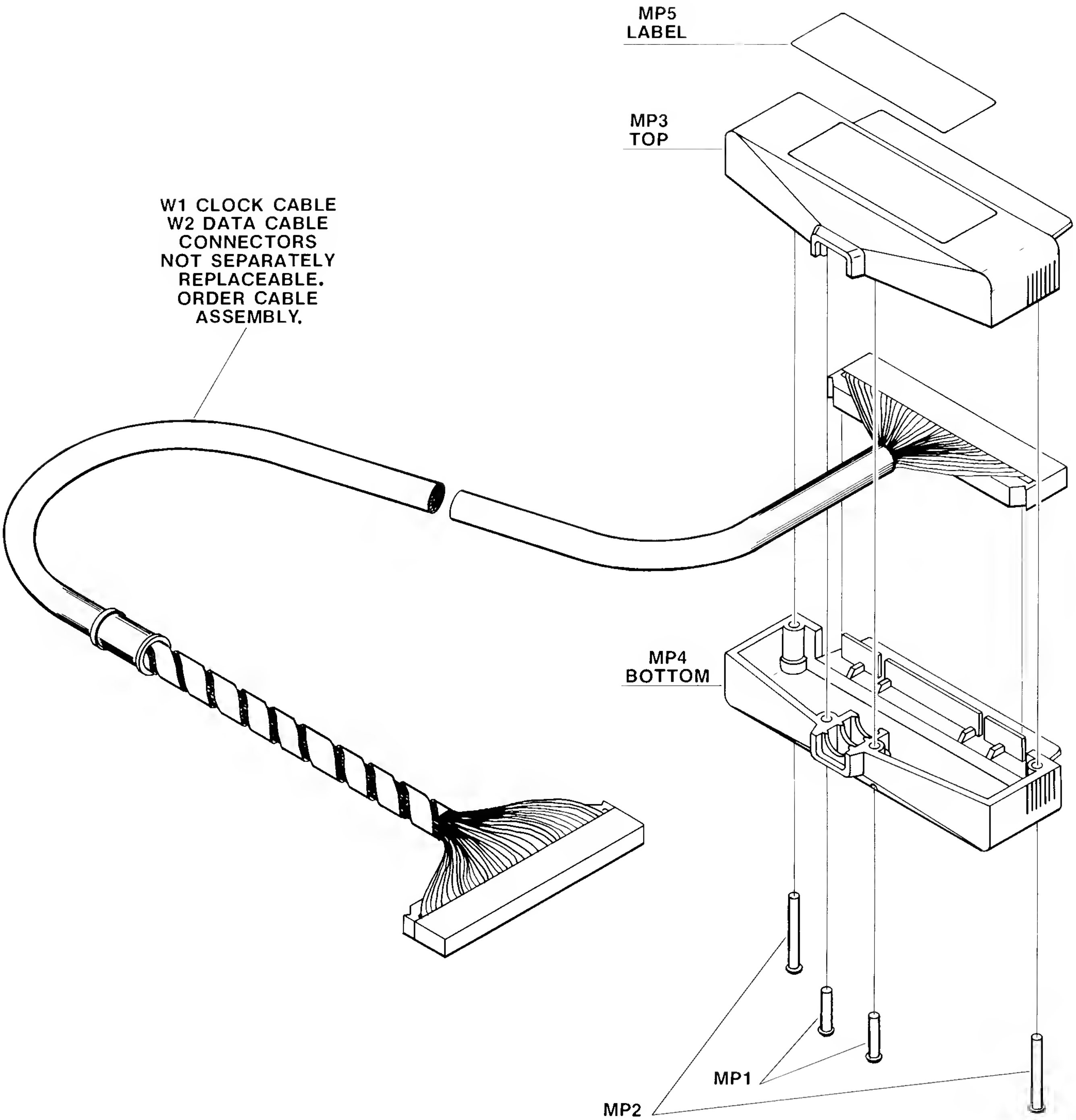


Figure 6-1. Probe Cable Breakdown

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64621A	3		STATE ANALYSIS CONTROL	28480	64621A
A1	64621-66503	7	1	10MHZ STATE ANALYSIS CONTROL BOARD	28480	64621-66503
A1C1	0160-2055	9	50	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C5	0160-3793	4	3	CAPACITOR-FXD 680PF +-1% 100VDC MICA	28480	0160-3793
A1C6	0140-0149	6	4	CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A1C7	0140-0149	6		CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A1C8	0160-3067	5	1	CAPACITOR-FXD 200PF +-5% 300VDC MICA	28480	0160-3067
A1C9	0160-3793	4		CAPACITOR-FXD 680PF +-1% 100VDC MICA	28480	0160-3793
A1C10	0140-0149	6		CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A1C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C12	0160-3508	9	2	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C17	0160-3793	4		CAPACITOR-FXD 680PF +-1% 100VDC MICA	28480	0160-3793
A1C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C36	0160-0178	3	2	CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-0178
A1C37	0160-0178	3		CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-0178
A1C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C46	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C48	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C49	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C50	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C52	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C53	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C54	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C55	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C56	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C57	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C58	0180-1746	5	6	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C59	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C60	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C61	0140-0149	6		CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A1C62	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C63	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C64	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C65	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C66	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C67	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C68	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1CR1	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1J3	1251-7005	3	1	CONNECTOR 50-PIN M POST TYPE	28480	1251-7005
A1MP1	64621-85001	0	1	EXTRACTOR P.C. BOARD	28480	64621-85001
A1MP2	64621-85002	1	1	EXTRACTOR-P.C. BOARD	28480	64621-85002
A1MP3	1480-0116	8	1	PIN-GRV .062-IN DIA .25 IN LG STL	28480	1480-0116
A1Q1	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1R1	0757-0394	0	12	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R2	0698-6612	1	20	RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R3	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R4	2100-3123	0	8	RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R5	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R6	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R7	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R8	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R9	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R10	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R11	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R12	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R13	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R14	0757-0346	2	4	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1R15	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1R16	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1R17	0698-3445	2	1	RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
A1R18	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1R19	0698-3455	4	2	RESISTOR 261K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2613-F
A1R20	0698-3154	0	2	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A1R21	0698-3152	8	1	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A1R22	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A1R23	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R24	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R25	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R26	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R27	0757-0437	2	2	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1R28	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1R29	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R30	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R31	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R32	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R33	0757-0438	3	3	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R34	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R35	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R36	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R37	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R38	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R39	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R40	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R41	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R42	0757-0726	2	1	RESISTOR 511 1% .25W F TC=0+-100	24546	C5-1/4-T0-511R-F
A1R43	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R44	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R45	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R46	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R47	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R48	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R49	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R50	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R51	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R52	0698-3455	4		RESISTOR 261K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2613-F
A1R53	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-100	28480	0698-6612
A1R54	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R55	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R56	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R57	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1TP2	0360-0535	0	13	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP14	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
GND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
GND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
GND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP18	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP19	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U1	1NB4-5010	3	1	IC, STATE ANALYZER CONTROLLER	28480	1NB4-5010
A1U2	1810-0273	9	9	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U3	1810-0298	8	12	NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U4	1820-2359	7	2	IC MISC ECL 14-INP	07263	F10014PC
A1U5	1820-1400	7	3	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A1U6	1820-0802	1	4	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U7	1820-2359	7		IC MISC ECL 14-INP	07263	F10014PC
A1U8	1820-0269	4	2	IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
A1U9	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U10	1810-0280	8	3	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A1U11	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A1U12	1810-0302	5	2	NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A1U13	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U14	1820-1201	6	1	IC GATE TTL AND QUAD 2-INP	01295	SN74LS08N
A1U15	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U16	1820-1831	8	2	IC GATE ECL OR QUAD 2-INP	04713	MC10103L
A1U17	1820-1708	4	6	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U18	1820-1708	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U19	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U20	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U21	1820-1944	4	2	IC LCH ECL D-TYPE POS-EDGE-TRIG DUAL	04713	MC10130L
A1U22	1820-1944	4		IC LCH ECL D-TYPE POS-EDGE-TRIG DUAL	04713	MC10130L
A1U23	1820-0817	8	1	IC FF ECL D-M/S DUAL	04713	MC10131P
A1U24	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A1U25	1NB4-5018	1	1	IC, CLOCK GENERATOR	28480	1NB4-5018
A1U26	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
A1U27	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A1U28	1826-0271	0	2	IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U29	1826-0271	0		IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U30	1826-0544	0	1	V RFF 8-DIP-C	04713	MC1403U
A1U31	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U32	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U33	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U34	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U35	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U36	1816-1462	2	4	IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A1U37	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U38	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A1U39	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U40	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A1U41	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U42	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A1U43	1820-0806	5	1	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A1U44	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U45	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A1U46	1810-0219	3	4	NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
A1U47	1820-0809	8	2	IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U48	1810-0219	3		NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
A1U49	1810-0219	3		NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
A1U50	1820-0809	8		IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A1U51	1810-0219	3		NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
A1U52	1820-1173	1	6	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U53	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U54	1826-0856	7	2	IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A1U55	1826-0856	7		IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A1U56	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U57	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208B470
A1U58	1816-1338	1	4	IC ECL/10K 64-BIT STAT RAM 6-NS	07263	10145APC
A1U59	1816-1338	1		IC ECL/10K 64-BIT STAT RAM 6-NS	07263	10145APC
A1U60	1816-1338	1		IC ECL/10K 64-BIT STAT RAM 6-NS	07263	10145APC
A1U61	1816-1338	1		IC ECL/10K 64-BIT STAT RAM 6-NS	07263	10145APC
A1U62	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U63	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U64	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U65	1820-1052	5	10	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U66	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U67	1820-1997	7	6	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U68	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U69	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U70	1816-1308	5	8	IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U71	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U72	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U73	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U74	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U75	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U76	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U77	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U78	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U79	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U80	1820-1831	8		IC GATE ECL OR QUAD 2-INP	04713	MC10103L
A1U81	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U82	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U83	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U84	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U85	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U86	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U87	1820-1428	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U88	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U89	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U90	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U91	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U92	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U93	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U94	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U95	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U96	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U97	1820-1282	3	4	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A1U98	1820-1282	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A1U99	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U100	1820-1216	3	3	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U101	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U102	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U103	1820-1282	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A1U104	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U105	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U106	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A1U107	1820-1282	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A1U108	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U109	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U110	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U111	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U112	1NB4-5009	0	1	IC, COUNTER 20 BIT GRAY CODE	28480	1NB4-5009
A1U113	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U115	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U116	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A1U117	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U118	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A1U119	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A1U120	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U121	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A1U122	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U123	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A1U124	1820-0269	4		IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
A1U125	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U126	1820-0780	4	1	IC DRVR TTL LINE DRVR QUAD	27014	DS8831N
A1U127	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U128	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U129	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U130	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1XU1	1200-0654	7	3	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU25	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU26	1200-0639	8	2	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU28	1200-0796	8	2	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1XU29	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1XU47	1200-0607	0	4	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU50	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU53	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU70	1200-0612	7	8	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU71	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU72	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU73	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU90	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU91	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU92	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU93	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU112	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU117	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU126	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU127	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP1	2200-0147	4	2	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP2	2200-0151	0	2	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP3	64620-67601	7	1	HOOD-CONNECTOR ASSEMBLY (TOP)	28480	64620-67601
MP4	64620-67602	8	1	HOOD-CONNECTOR ASSEMBLY (BOTTOM)	28480	64620-67602
MP5	7121-2158	8	1	CABLE-CLOCK PROBE	28480	7121-2158
W1	64620-61602	6	1	CABLE-CLOCK ASSEMBLY NOTE IF THE CABLE IS DAMAGED, THE ENTIRE W1 CABLE-CLOCK ASSY MUST BE REPLACED.	28480	64620-61602
W2	* *	*	*	CABLE-DATA ASSEMBLY ** DEPENDS ON THE NUMBER OF ACQUISITION BOARDS BEING USED IN THE SYSTEM. SEE THE ACQUISITION MANUALS.	28480	* *
W3	64620-61605	9	1	CABLE-SYNCHRONOUS EXPANSION BUS (SEB)	28480	64620-61605
W4	64620-61620	8	1	CABLE - INTERMODULE BUS (IMB)	28480	64620-61620

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
S0167	FUJITSU LTD	TOKYO JP	
S4013	HITACHI	TOKYO JP	
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94042
11236	CTS OF BERNE INC	BERNE IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
20932	EMCON DIV ITW	SAN DIEGO CA	92129
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
25403	AMPEREX ELEK CORP SEMICON & MC DIV	SLATERSVILLE RI	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE CA	94086
52763	STETTNER-TRUSH INC	CAZENOVIA NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA PA	19108

See introduction to this section for ordering information

SECTION VII

MANUAL BACKDATING

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific repair number prefix.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the repair number prefix shown on the manual title page. If the repair prefix is not the same as the one on the title page, find your repair number prefix in Table 7-1 and make the changes to the manual that are listed for that repair number prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1,2 and 3 are required for your repair number, do change 3 first, then change 2, and finally change 1.

7-5. If the repair number of your instrument is not listed either on the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Manual Changes

PREFIX	MAKE CHANGES
2144A	1 and 2
2246A	2

CHANGE 1

Section VI,

Page SAC 6-4, Table 6-2. Replaceable Parts List,

Change A1 part number from 64621-66502 to 64621-66501. Check digit from 6 to 5.

Page SAC 6-5, Table 6-2. Replaceable Parts List,

Change A1R2, R3, R9, R10, R29-31, R36-41, R43-47, R51, R53 part numbers from 0698-6612 to 0757-0283 (20 places). Check digit from 1 to 6 (20 places). Tolerance from 0.1% to 1% (20 places). Mfr Code from 28480 to 24546. Mfr Part Number from 0698-6612 to C4-1/8-TO-2001-F.

Delete last line -A1TP18, 0365-0535, 0, Terminal Test Point PCB, 00000, Order by Description.

Change A1TP2 QTY from 12 to 11.

CHANGE 2

Section VI,

Page SAC 6-4, Table 6-2. Replaceable Parts List,

Change A1 to read: A1, 64621-66502, 6, 1, 10MHZ STATE ANALYSIS CONTROL BOARD, 28480, 64621-66502.

Delete A1C68, 0160-2055, 9, -, CAPACITOR-FXD .01UF +80-20% 100VDC CER, 28480, 0160-2055.

Change A1C1 QTY from 50 to 49.

Page SAC 6-5, Table 6-2. Replaceable Parts List,

Delete A1TP19, 0360-0535, 0, -, TERMINAL TEST POINT PCB, 00000, ORDER BY DESCRIPTION.

Change A1TP2 QTY from 13 to 12.

Page SAC 6-6, Table 6-2. Replaceable Parts List,

Delete A1U14, 1820-1201, 6, 1, IC GATE TTL AND QUAD 2-INP, 01295, 1820-1201.

Section VIII,

Delete TP19 from the eight component locators facing the schematics.

Service Sheet 5,

Remove U14C.

Disconnect U1 pin 17 from U14C pins 9 and 10.

Disconnect U14C pin 8 from J2 pin 43. Show pin 43 as NC.

Disconnect J2 pins 42 and 44 from ground. Show them as NC.

Service Sheet 7,

Show U98A pins 2, 3, and 4 as no connection (NC).

Disconnect U73 pin 9 from U73 pin 17 (+5V).

Connect U73 pin 9 to U73 pin 11 (LSFLGB).

Service Sheet 8,

Delete C68 from the list of +5 Volt bypass caps (.01UF).

Delete TP19, SA START/STOP, test point from P1 pin 69.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains information for troubleshooting and repairing the Model 64621A State Analysis Control Board.

8-3. The block diagram, schematic, component location figure, and other service information are provided on fold-out service sheets to help you in servicing the Model 64621A.

8-4. Because the State Analysis Control is software dependent, it becomes very difficult to discuss the Theory of Operation at the bit level. Therefore, the following discussion is at the concept level of various functions.

8-5. The following five areas of the State Analyzer are discussed in detail: 1. Clock Term Generator, 2. Strobe Generator, 3. Sequencer, 4. Analysis Controller, and 5. State/Time Counter.

8-6. The Clock Term Generator, Analysis Controller, and the State/Time Counter are custom integrated circuits manufactured by Hewlett - Packard. How the ICs work is presented to help you understand how the State Analyzer works, rather than a "black box" approach.

8-7. The Strobe Generator is discussed because it must be repaired using conventional methods instead of Signature Analysis.

8-8. The Sequencer is discussed because it is not apparent from the schematics how it works, due to feedback loops.

8-9. STATE ANALYZER SUBSYSTEM BLOCK DIAGRAM.

8-10. The State Analysis Subsystem Block Diagram, Figure 8-1, is designed to give an overview of the State Analysis System. The block diagram is divided into two sections, the Control Board and the Data Acquisition Board. The Data Acquisition Board is also divided into two sections, the Overview block, which is only on the 20 channel board, and the rest of the blocks which are on both the 20 channel and 40 channel boards.

8-11. The shaded blocks on the Control Board are all parts of the Analysis Controller (U1) a hybrid chip. Other hybrids are the Clock Term Generator (U25), the Trace State/Time Counter (U112) on the Control Board, and the Counter (U23) in the Overview State/Time Counter on the 20 channel board.

8-12. The Block Diagram is also divided into six sections shown by the red lines. These six secitons represent time. There are six time periods; 1. Clock Qualification, 2. Input Data Sampled, 3. Decode Trigger Terms and Bucket Generation, 4. Pipeline Registers, 5. Data Storage/Count Enable Determination, and 6. Store Data and Output.

8-13. DESCRIPTION.

8-14. Time Period 1.

8-15. Clock Qualification consists of all the circuitry for setting up the threshold levels for the clock. The Data Threshold block sets up the threshold levels for the 20 channels of data. In addition to the clock threshold circuitry, the Control Board portion of this section contains the interfaces to the general purpose preprocessor, the interface to the Inter Module Bus (IMB), and the Clock Term Generator. The Clock Term Generator is loaded by the CPU when the clock is specified in the format specification. When that specification is satisfied the Clock Term Generator sends out a 15ns pulse to the Strobe Generator which initiates a timing sequence in the rest of the state analyzer.

8-16. Time Period 2.

8-17. The key to the State Analysis System is the Strobe Generator. It provides all the timing signals for the system to insure the proper sequence of events.

8-18. The Strobe Generator, in Time Period 2, is where the input data is latched into the acquisition cards. The signals from the Strobe Generator, P/NBSRS (Positive/Negative Bus State Recognition Strobe), are sent across the SEB (Synchronous Expansion Bus) to strobe in the data on the acquisition cards. The PBSRS signal is also used in the Overview State/Time Counter (only on the 20 channel acquisition board) to increment the overview counter every time a valid clock term is encountered.

8-19. Time Period 3.

8-20. The Resource Pattern, Sequence Pattern and Event Generation is where the State Analyzer's resources are allocated and the Sequencer patterns determined. The Acquisition Board detects specified combinations of trigger, storage, and count information, and sends that information on LBRP0-7 (Low Bus Resource Pattern) over the SEB to the Resource Allocation portion of the Analysis Controller. This section of the Analysis Controller determines, from the data on the LBR0-7 lines, how to allocate the set number of resources available to the state analyzer among the trigger, storage, and count specifications.

8-21. The Resource Pattern, Sequence Pattern and Event Generation block also determines when the Data Acquisition boards have found the sequence state(s) requested by the user. If no sequence events were specified, then the Low Bus Sequence Pattern 0-3 (LBSP 0-3) lines would always be high.

8-22. Time Period 4.

8-23. Time Period 4, Pipeline Registers, is where the State Analyzer latches all the data so that the front end can bring in new data, and the rest of the analyzer can process the current data. The latching is done by the Positive Pipeline Strobe (PPLS) which occurs 95ns after the Strobe Generator is started. This allows the state boards to work on 2 different sets of input data at the same time. The timing for PPLS is critical.

8-24. Time Period 5.

8-25. The Data Storage/Count Enable Determination continues the resource allocation and gating that was started in time period 4. All this is done on the control board in the Analysis Controller. These control signals are output by the Analysis Controller gating functions:

HOVCQ - (High Overview Count Qualify)

HOVCQ, when high, enables the overview counter in the 20 channel Data Acquisition Board. It is derived from the internal Overview Count Signal or LSOCE (Low Sequence Overview Count Enable) from the Sequencer.

HCQ - (High Count Qualify)

When high, HCQ enables the Trace State/Timing Counter allowing it to increment. It is derived by the internal Trace Count signal or the LSCE (Low Sequence Counter Enable) signal from the Sequencer.

LSFLG - (Low Store Flag)

This active low signal indicates to the Trace Count/Status Memory that storage is enabled. LSFLG is enabled by the internal storage signal, or LSE (Low Storage Enable) from the IMB (Inter Module Bus), if active, or either of the signals from the Sequencer, LSSE/Q (Low Sequence Store Enable/Qualify).

NTRIG - (Negative Trigger)

This signal goes from a high to a low each time a user specified trigger event occurs. It is used to latch signals into the trace point latch internal to the Analysis Controller, and into the BNC Port latch. It is derived from the internal Trigger Signal, or LSTE/HSRS (Low Sequence Trigger Enable/High State Recognition Strobe) signals from the Sequencer, or either LTE/HTR (Low Trigger Enable/High Trigger) from the IMB.

LTE - (Low Trigger Enable)

This active low bidirectional signal is the IMB signal that is sent to the other modules when a trigger is recognized by the control board. It is derived from the same signals NTRIG output is derived from.

8-26. The Trace State/Time Counter in Time Period 5 is used whenever that function is turned on in the trace specification. It is another of the hybrid chips designed for this instrument. Its function is to count the number of states between two states or periods of time between two states. When LSTATE (Low State) is low the counter counts the number of states between two stored states. The counter is incremented by PINC (Positive Increment) which is developed from HWQ (High Write Qualify) and HWRT (High Write). HWQ is generated by the Analysis Controller, and is used to disable the counter when the output of the Counter is being stored in the Trace Count/Status Memory. HWRT is developed in the Strobe Generator each time a qualified clock is detected.

8-27. When LSTATE is high the Counter counts the time between two states. The L25 MHz (Low 25 Megahertz) signal is used to clock the Counter in this mode.

8-28. Time Period 6.

8-29. Time Period 6 is the Store Data and Output block. This is the last stage before the captured data and count information is sent to CPU for display. There are three separate operations that occur in this block.

8-30. The first is on the 64623A (the 20 channel acquisition board) where the Overview events are stored in the Overview memory. The CPU unloads Overview Memory using LRDL (Low Read Data Latch), for the Overview Event Data Latch, and LRDOV (Low Read Overview), for the Overview Memory Address Counter Latch.

8-31. The second operation that occurs in this block is on both the 64622A (40 channel acquisition board) and the 64623A (20 channel acquisition board). The 20 channels of data on each half of the board are latched into the Trace Pod Data Memory by HBQWRT (High Bus Qualified Write). HBQWRT synchronizes the data storage with the Trace Counter/Status Memory on the control board. The data is read from the Trace Pod Data Latch onto the CPU Data Bus by LRDL (Low Read Data Latch) which is developed on the acquisition board from CPU control signals.

8-32. The third operation takes place on the control board. The Trace Count/Status Memory section of the Control Board stores the 8 outputs of the Sequence State Latch/Counter (TSS0-7), the 20 outputs of the Trace State/Time Counter (CNT0-19) and three control signals HOTFB (High Overview Trigger Flag Buffered), HCQB (High Count Qualify Buffered), and LSFLGB (Low Store Flag Buffered). The CPU needs these control signals to interpret the data from the state system.

8-33. The final section is the five registers that hold the information to be read onto the CPU Data Bus. These five registers are enabled by control signals developed in the CPU Read Decoder on the Control Board from the CPU Address Bus signals. The five signals are:

LRSQRG - (Low Read Sequence Register)

This active low signal allows the output of the Sequence State Latch/Counters (TSS 0-7) to be read onto the CPU Data Bus.

LRTDR - (Low Read Trace Data Register)

When low, LRTDR enables the Trace Point Register allowing the value of the Trace Count/Status Memory to be read by the CPU.

LRTPRG - (Low Read Trace Point Register)

This active low signal allows the Trace Point address to be read over the CPU Data Bus. The Trace Point address was latched by LTRCP when the trace point was found.

LRSTS - (Low Read Status)

When low, LRSTS enables the Analysis Status Buffer to allow eight different signals to be read by the CPU.

Figure 8-1.
State Analyzer Subsystem Block Diagram

8-34. CONTROL BOARD BLOCK DIAGRAM.

8-35. The Model 64621A State Analysis Control Board consists of the following nine basic functional groups:

* Clock Probe Interface
* Preprocessor Interface Bus
* Strobe Generator
* Sequencer
* Analysis Controller
* BNC Control
* Trace State/Time Counter
* Trace Count/Status Memory
* Mainframe Interface

8-36. CONTROL BOARD BLOCK DIAGRAM THEORY.

8-37. CLOCK PROBE INTERFACE.

* The Clock Probe Interface consists of the Clock Term Generator chip, U25, and the D/A Converters, U54 and U55.

* The Clock Term Generator allows eight different clocks to be input to the State Analyzer.

* The eight clocks may be used in various qualification patterns.

* The Clock Term Generator outputs a master clock to the Strobe Generator.

* The D/A Converters provide threshold levels for the Clock Probe. The threshold levels are set by the operator through the keyboard.

8-38. PREPROCESSOR INTERFACE BUS.

* The Preprocessor Interface Bus provides the communications path from the Mainframe to the General Purpose Probes and the General Purpose Preprocessor.

* The clock for the State Analyzer is provided by the Preprocessor when it is being used instead of the Clock Probe.

8-39. STROBE GENERATOR.

* The Strobe Generator converts the output of the Clock Term Generator, U25, into the various strobes needed throughout the State Analyzer (including the Acquisition Boards).

* The amounts of delay for each strobe and the pulse widths are adjustable.

* The Strobe Generator can also be activated by the Mainframe Interface for Performance Verification using signals PPVSTB or PBSRQ.

8-40. SEQUENCER.

* The Sequencer is a group of counters, memories, and gates that allow the State Analyzer to find events in various sequences and occurrences.

* The Sequencer is programmed by the Mainframe for each Trace to be performed. Variables are entered from the keyboard.

8-41. ANALYSIS CONTROLLER.

* The Analysis Controller, U1, is the heart of the State Analyzer.

* The Analysis Controller recognizes events occurring on the Acquisition Boards and in general provides the handshaking between the Acquisition Boards and the Control Board.

* The Analysis controller is programmed by the Mainframe CPU.

* The Analysis Controller controls the Intermodule Bus (IMB).

8-42. BNC CONTROL.

* The BNC Control circuit drives signals of correct polarity to the Mainframe's Rearpanel.

* The polarity is selected by software.

8-43. TRACE STATE/TIME COUNTER.

* The Trace State/Time Counter, U112, is a 20 bit floating point gray code counter.

* The State/Time Counter accumulates the time between two stored states, or the number of states between two stored states.

* The State/Time Counter is referenced to a 25 MHz crystal when measuring time, and to the qualified count states as input in the trace specification when counting states.

* The 25 MHz crystal is located in the Mainframe.

8-44. TRACE COUNT/STATUS MEMORY.

* The Trace Count/Status Memory stores the values output from the Trace State/Time Counter for each measurement.

* The Trace Count/Status Memory can store values for each of the 256 locations in the Trace Pod Data Memory on the Acquisition Boards.

* The values are read from the memories over the Mainframe's Data Bus and formatted by the CPU for display on the CRT.

* The Trace Count/Status Memory stores sequence states and flags associated with each counter value.

8-45. MAINFRAME INTERFACE.

* The Mainframe Interface consists of various latches and buffers (wire ORed) for interfacing the State Analyzer's circuits to the Mainframe.

* Through the use of read and write decoders, the Mainframe can select various groups of circuitry on the Control Board and write to (program) or read from (verify, interrogate) them over the Mainframe's Data Bus.

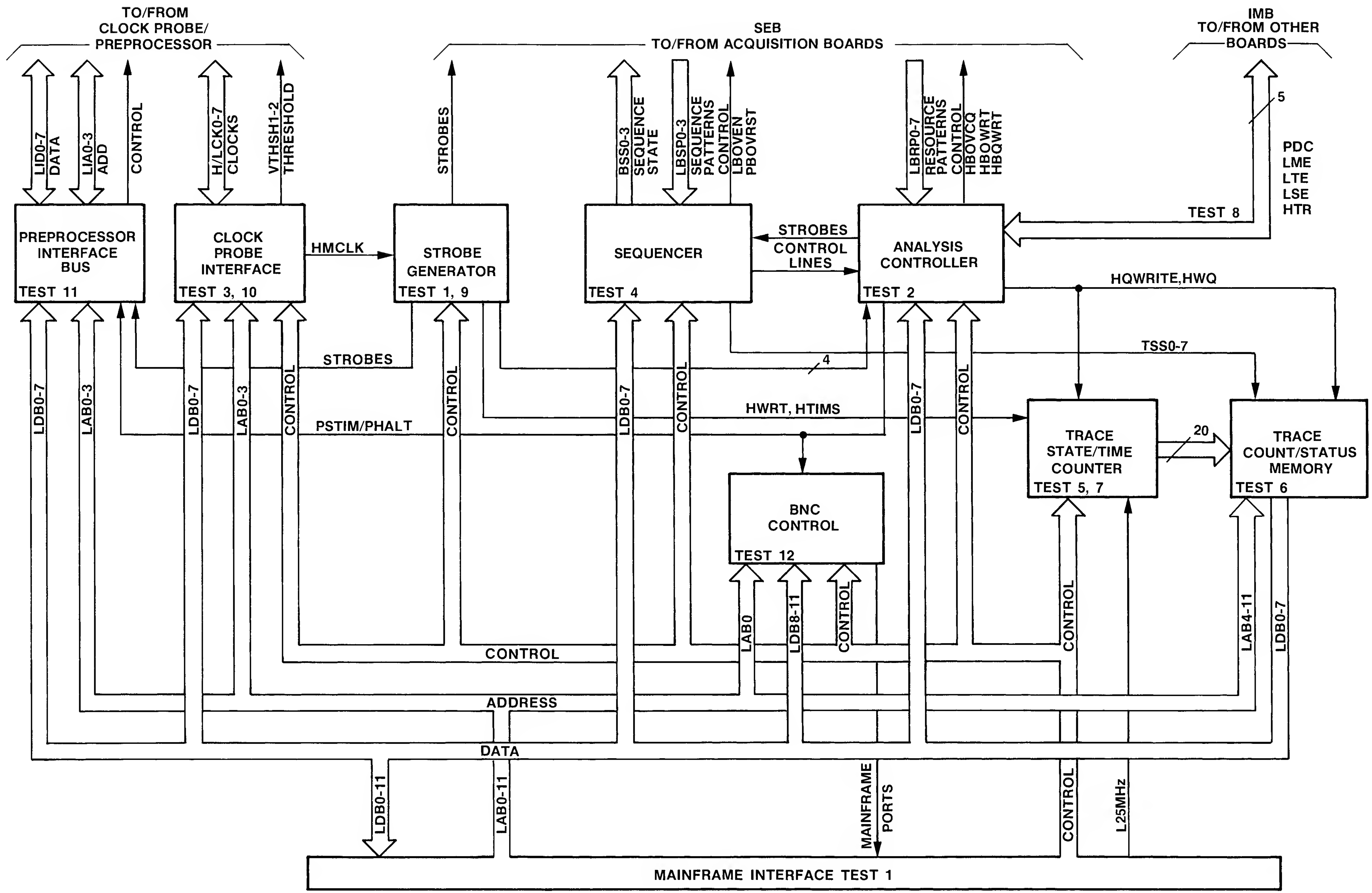


Figure 8-2.
State Analysis Control Board Block Diagram

8-46. DETAILED CIRCUIT THEORY.

8-47. CLOCK TERM GENERATOR.

8-48. The Clock Term Generator, U25, is a custom designed clock decoder. It converts eight clock channel inputs into a single master clock.

8-49. Each clock input can be programmed by loading two internal shift registers. The shift register outputs set up the channel to be edge sensitive or level sensitive, but not both at once. The level sensitive inputs are called clock qualifiers and are wire ANDed internally. Any combination of inputs can be made edge sensitive, and any input can trigger on a positive edge, a negative edge, or both edges.

8-50. The eight clock channel inputs are differential at approximately ECL levels, and the master clock output (HMCLK) is ECL. The two shift registers and their clock are TTL levels.

8-51. Clock Term Generator Timing.

8-52. Inputs used as clock qualifiers have a set-up time of 20 nS and hold time of 0 nS. Inputs used as clocks must have a pulse width of 20 nS minimum. Due to system restrictions, the master clock rate is 10 MHz maximum. Propagation delay is approximately 8 nS from clock input to master clock output.

8-53. Clock Term Generator Block Diagram.

8-54. Prior to execution of a trace, the Edge Detect Register and Level Select Register are loaded from lines DB0 and DB1 using Positive Write Clock (PWCLK). Two bits per clock channel control the channel's Level Select Gate. The channel can be made "don't care" by programming both bits high. The outputs of all eight Level Select Gates are ANDed, so that all qualifiers must be true before the data input to the Edge Detect filp-flops go true.

8-55. Two more programmable bits per clock channel are needed to control which clock edge, if any, will produce a High Master Clock (HMCLK). A high output by the Edge Detect Register to any flip-flop will prevent that detector from toggling. All filp-flop outputs are ORed to produce HMCLK. Therefore, all possible combinations of channels and edges are allowed. The only restriction is that HMCLK pulses must be at least 100 nS apart.

8-56. HMCLK drives Pulse Width Output (PWO) which is connected externally to Pulse Width Input (PWI). After a delay, PWI resets the edge detector responsible for the master clock. This results in a pulse width of 15 nS maximum for HMCLK.

8-57. The Edge Detect Shift Register and Level Detect Shift Register can be made to overflow during performance verification. These registers output High Clock Data 0 and 1 (HCD0-1).

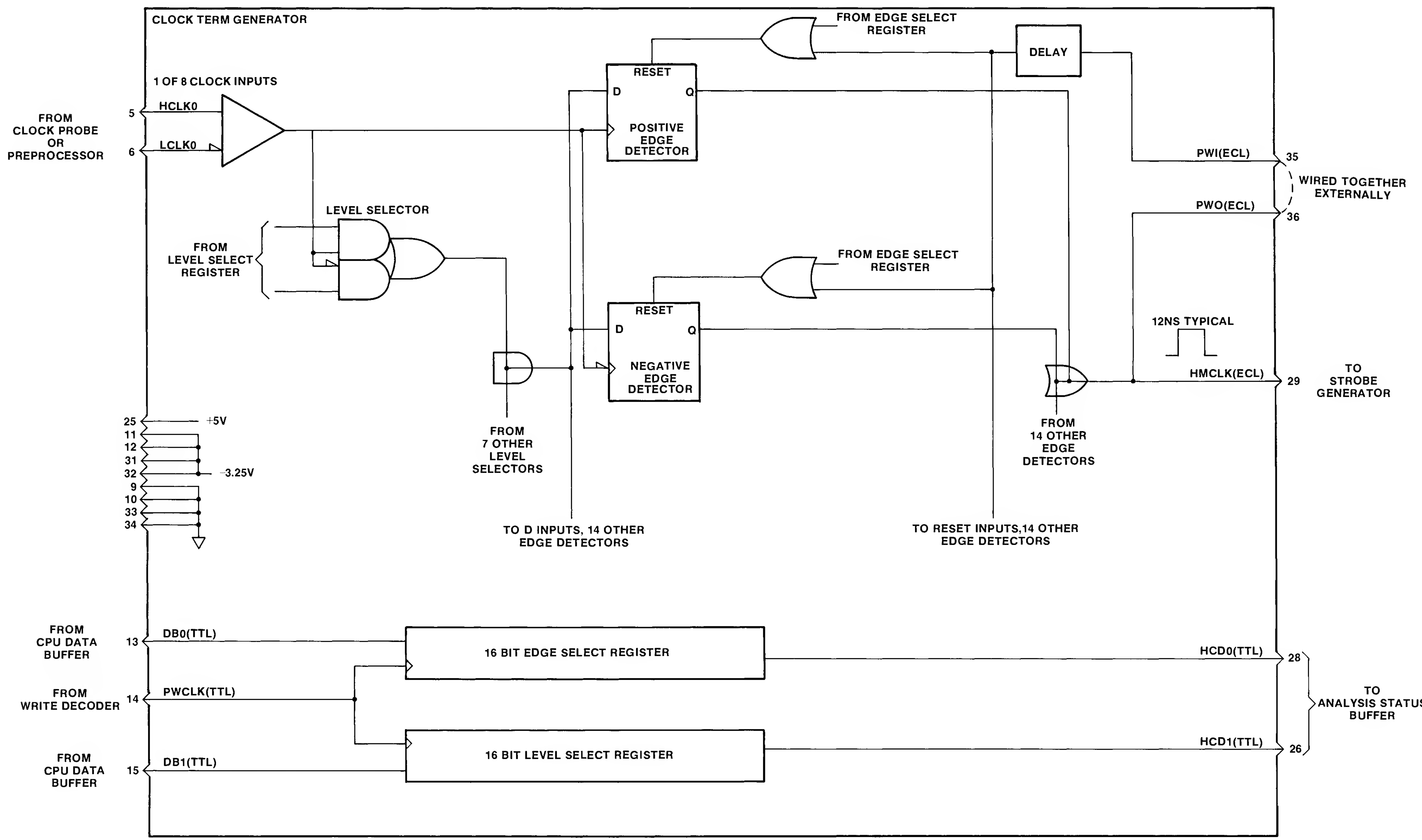


Figure 8-3.
Clock Term Generator Block Diagram

8-58. STROBE GENERATOR.

8-59. The Strobe Generator develops seven major strobes from HMCLK or PPVSTB and PBSTBRQ (see Figure 8-4);

1. HSRS 2.HTIMS 3. HOVS 4. HPLS 5. HWRT 6. LMV 7. LDV

HMCLK is used to drive the Strobe Generator in the Analyzer's run mode. PPVSTB and PBSTBRQ are used in the Performance Verification mode.

8-60. Strobe Uses.

8-61. HSRS is used to clock the IMB State Recognition Register in the Analysis Control Chip. P/NBSRS clocks data into the State Recognition Latch/Counters on the Data Acquisition Boards.

8-62. HTIMS is used to transfer information to the outputs of the Trace State/Time Counter.

8-63. HOVS is used to develop LBOVEN and PBOVRST. LBOVEN and PBOVRST are used on the 20 Channel Data Acquisition Board only. LBOVEN allows the Overview section to look for its trigger events. PBOVRST is used to reset the Overview State/Time Counter.

8-64. HPLS is used to latch information into the Pipeline Registers on the Control Board and the Data Acquisition Boards.

8-65. HWRT is used to time write commands to Trace and Overview Memories. These write commands store data in the Memories.

8-66. LMV develops P/NMACRS. P/NMACRS is used to latch information from the Trace Count/Status Memory Address Counter into the Trace Memory Address Counter Read Register.

8-67. LDV is used to indicate the point in time that the Trace Memory outputs are stable.

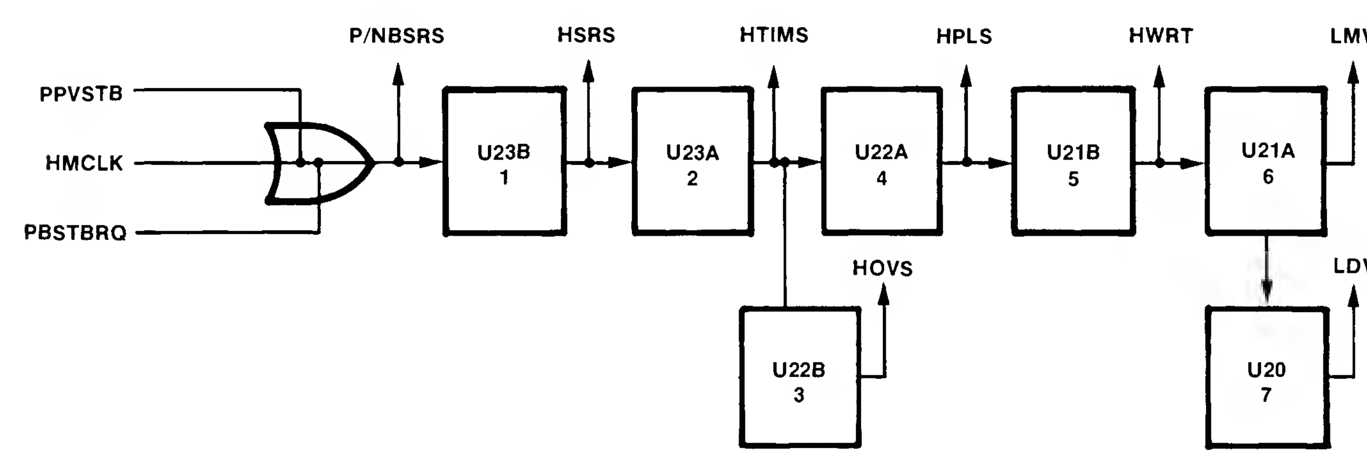


Figure 8-4. Strobe Generator Block Diagram

8-68. How A Strobe Is Generated.

8-69. Figure 8-4 is a simple block diagram of the Strobe Generator, and Figure 8-5 shows the timing relationship of the seven major strobe signals. The time periods indicated are approximate values and should not be used for calibration purposes.

8-70. Six of the seven stages work very much the same. Therefore, only the first stage will be discussed. The seventh stage is built using OR gates.

8-71. At time zero, U23 pin 11 goes from a low to a high (the same in the run mode or Performance Verification mode). Because U23 pin 10 is connected to a high level, U23 pin 15 goes high when the positive edge on pin 11 occurs. At the same time, U23 pin 14 begins to go low. Pin 14 cannot go low instantly due to the charge in C10 and the currents in R18, R8 and the 240 ohms in U9. The amount of time it takes pin 14 to reach a low state is determined by these components.

8-72. The hysteresis of U50 pin 13 is set to -1.55 V by U50 pin 9, two 220 ohm resistors in U51, and one 240 ohm resistor in U35. As U50 pin 13 (U23 pin 14) goes negative (the hysteresis level being crossed), U50 pin 15 goes positive, changing the hysteresis level. This action is fed back to U50 pin 12 and enhances U50 pin 13 going negative, causing U50 pin 15 to change to a high state very quickly.

8-73. The output of stage one, U50 pin 15, is fed to the next stage, providing U23 pin 6 with a positive going clock. The same action as in stage one now begins in stage two. This effect ripples through the remaining stages.

8-74. The output of U50 pin 15 is also sent back to the reset input, of U23B pin 13. When U50 pin 15 goes high, U23B is reset, causing U23 pin 15 to go low. This action defines the pulse width of HSRS.

8-75. At the same time, U23 pin 14 is going high at the rate defined by the RC network. When U50 pin 13 reaches the positive hysteresis U50 pin 15 goes low. The reset mode (U23 pin 13) is now removed and stage one is ready to begin the cycle again.

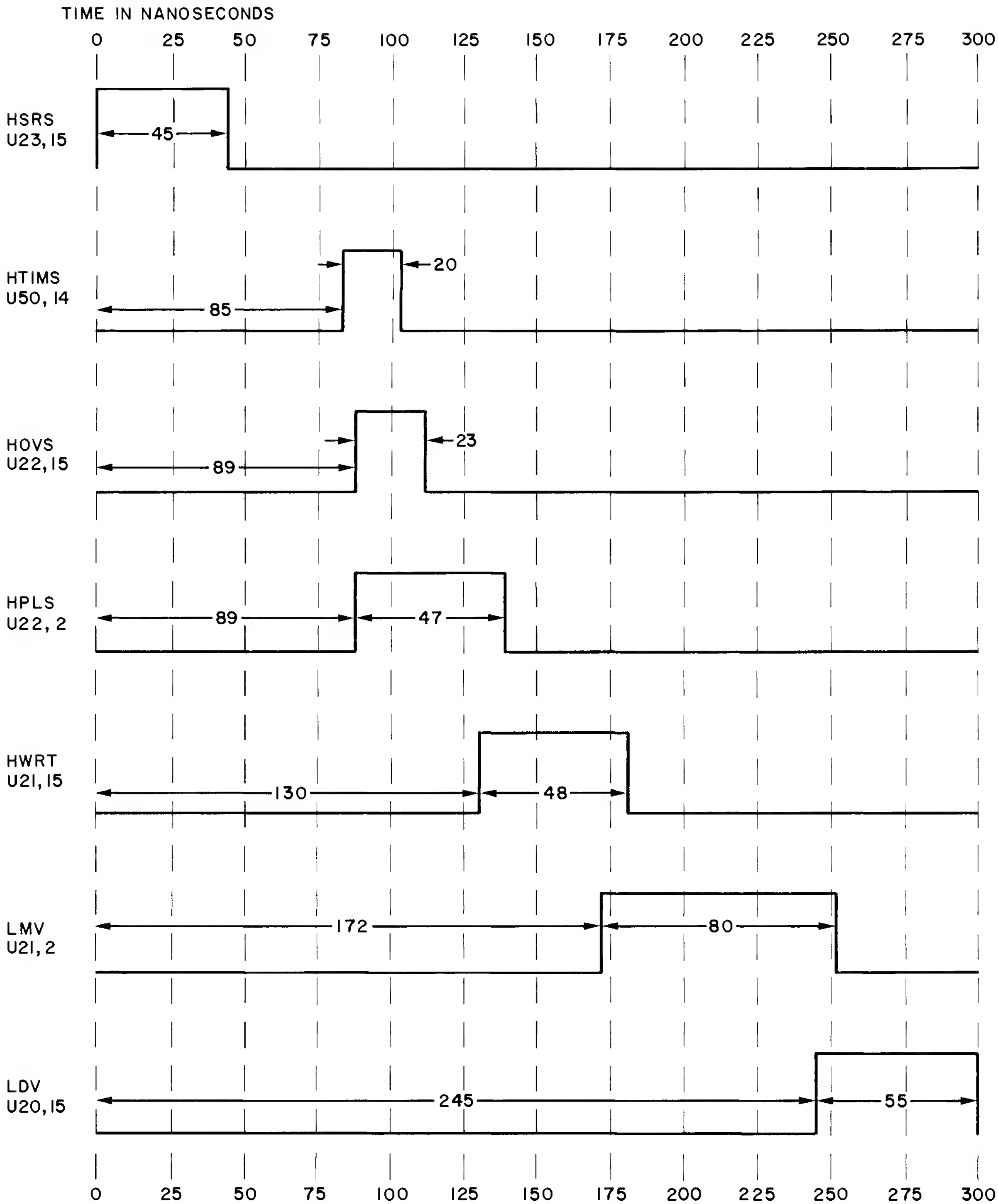


Figure 8-5. Strobe Timing Relationship

8-76. SEQUENCER.

8-77. Description.

8-78. The Sequencer consists of memories, counters and latches. Its purpose is to enable various functions of the State Analyzer Subsystem when a series of states or events have occurred in the system under test. The Sequencer hardware contains feedback circuitry which combines the sequence state with incoming data to form the next sequence state. The Sequencer is a good example of a synchronous state machine.

8-79. Functions.

8-80. The Sequencer can enable and disable all functions of the State Analysis Subsystem. See Figure 8-6. It can also cause the State Analyzer to trigger, store, and drive the IMB master enable. It must be loaded before execution of a trace or overview. To operate the Sequencer, the operator must specify a series of terms and/or windows. The terms usually represent states (e.g. an address or a data value) and the windows are an enable/disable pair of terms. Then the operator specifies the order in which these terms must occur, how many times each must occur (occurrence), and whether the next term must occur immediately or eventually. The operator must specify which sequence term will enable a function, and which term will disable a function. The operator may also specify which terms will restart the sequencer. Further details are available in the operator's manual.

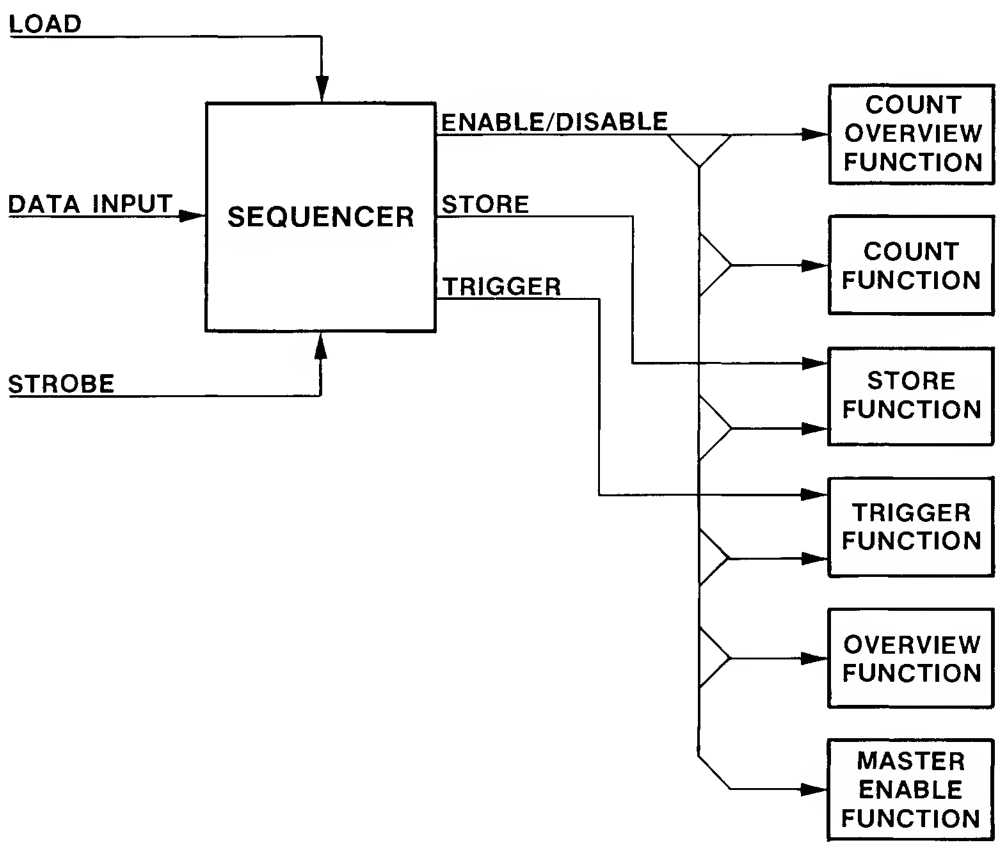


Figure 8-6. Sequencer Functions

8-81. Sequencer Specifications.

Depth 3 choices: 15 terms with restarts, no windows
7 terms with restarts, one window
3 terms without restarts, two windows

Occurrence 1 to 65535 times

Enable/Disable separately

Immediately/Eventually qualification

8-82. The depth is due to the feedback signals, Bus Sequence State (BSS0-3). Four signals allow only sixteen permutations, and one cannot be used. A window uses a signal, and it cannot be used by the terms. The Sequence Occurrence Counter is a sixteen bit counter.

8-83. Sequencer Block Diagram.

8-84. The major components of the Sequencer are the Sequence Pattern Trigger Memory, the Sequence State Latch/Counter, the Sequence Transistion Memories, the Sequence Occurrence Counter Memories, and the Sequence Occurrence Counter. All of these components are located on the Control Board except the Trigger Memories which are located on the Data Acquisition Boards. All the Memories must be loaded with information from the Mainframe before a trace begins.

8-85. During a trace, synchronous data (e.g. SYND0-19 on a 20 Channel Acquisition Board) from the State Recognition Latch/Counter provides part of an address to the Sequence Pattern Trigger Memory. The remainder of the address is provided by Bus Sequence State (BSS0-3), the last sequence state. The Trigger Memories output a sequence pattern (LBSP0-3). All Trigger Memories are wire ORed, and will drive a sequence pattern signal true (low) if all the Memories were loaded with a true state at the address supplied by the incoming data and the sequence state.

8-86. The sequence pattern is applied to the Sequence State Latch (this register is used as a counter only to load memories before a trace) after modification by the DME Gate. The DME, disjoint minterm event, is formed by inverting LBSP3 and ORing the result with LBSP2. This allows the operator to specify one term which has the form "ADDRESS <> 0FE5H". In other words, the operator can specify one "not equal to" term. Only LBSP0-2 are left as inputs to the Sequence State Latch.

8-87. BSS0-3 supplies four more inputs to the Sequence State Latch. BSS0-3 is output by the Sequence Transition Memories and forms the major feedback path for the Sequencer. The fourth input to the Latch is low Occurrence Carry (LOCCRY). LOCCRY is output by the Occurrence Counter when it has found a term the required number of times.

8-88. At Positive Pipeline Strobe (PPLS), these inputs are latched and applied to the Transition Memories, forming a new sequence state, named Trace Sequence State (TSS0-7). TSS0-7 is stored in Trace Memory and can be used by the operator to debug code. During performance verification, the CPU can read TSS0-7 from trace memory to verify proper functioning of the Sequencer.

8-89. The Sequence Transition Memories use TSS0-7 as address lines, and outputs 16 control signals. These signals include BSS0-3 used to change from one sequence state to the next, as well as function enables for count, trigger, store and master enable functions, a trigger signal (HSTR), and a store signal (LSSQ). The Memories also output Low Overview Enable (LOVEN) and Low Overview Reset (LOVRST) which control Overview on the 20 Channel Board. The Memories output two control signals to the Sequence Occurrence Counter; Low Sequence Occurrence Counter Load (LSOCLD) and Low Sequence Occurrence Counter Enable (LSOCEN).

8-90. **Function Enables.** The Sequencer will enable an Analyzer function only when all specified sequence terms have been found. The enabling signals serve as inputs to the Analysis Controller, except for LOVEN, and are as follows:

LSOCE	Low Sequence Overview Count Enable
LSCE	Low Sequence Count Enable
LSSE	Low Sequence Store Enable
LSTE	Low Sequence Trigger Enable
LOVEN	Low Overview Enable
LSME	Low Sequence Master Enable

The Sequencer can disable the above functions by driving any of them high.

8-91. **Sequence Occurrence Counter/Memories.** This part of the Sequencer controls the Occurrence, or, the number of times a sequence state must be found before the Sequencer moves on to the next specified state.

8-92. **An Example.** Suppose a state must occur 10 times before the Sequencer looks for the next state. Before the trace started, the Transition memories were loaded so that when the term prior to the 10 times term was found, the Transition Memories output Low Sequence Occurrence Counter Load (LSOCLD). At that time, BSS0-3 will cause the Occurrence Memories to output terminal count, 65535, minus 10, or 65525. LSOCLD will load the Occurrence Counter with 65526. The next time the sequence pattern goes true, the Transition Memories will output Low Sequence Occurrence Counter Enable, enabling the Occurrence Counter. The Occurrence Counter will be incremented by Positive Sequence Occurrence Counter Increment (PSOCINC) due to HWRT strobe. This will continue until the Counter reaches terminal count. Then the Counter outputs Low Occurrence Carry (LOCCRY), which will be latched into the Sequence State Latch and will change the sequence state.

8-93. **Sequencer Troubleshooting.**

8-94. Performance verification on the Control Board tests the Sequencer using Test 4. The loop includes the feedback paths of LOCCRY and BSS0-3. If signature analysis shows that multiple signatures are bad, it is due to the propogation of a bad signature around the loop. Test 1 has been provided to break the feedback. It is a stimulus test for the Sequencer which writes to all locations of the Transition Memories and the Occurrence Memories, and tests the Occurrence Counter, but does not latch the next sequence state into the Sequence State Latch.

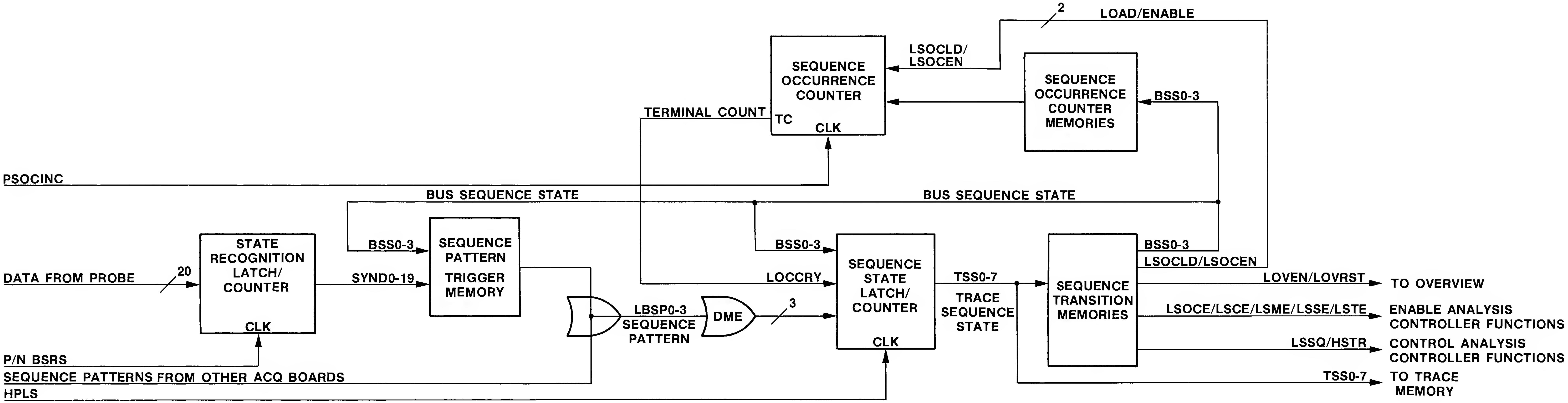


Figure 8-7.
Sequencer Block Diagram
SAC 8-18

8-95. ANALYSIS CONTROLLER.

8-96. Description.

8-97. The Analysis Controller, U1, is a custom designed IC which controls the master enable, count, store, and trigger functions of the State Analysis Subsystem. Figure 8-8 is a summary of the Analysis Controller.

8-98. The Analysis Controller decodes inputs from the Resource Patterns, the Sequencer and the Inter Module Bus (IMB), and outputs control signals to all cards in the State Analysis Subsystem and to other Analysis Subsystems over the IMB. The Analysis Controller must be programmed (loaded) before each execution. Electrically, the inputs and outputs are at ECL levels, with the exception of the following TTL signals: NTR, NMC, LLOAD, SERDATA, PLCLK, and LRUN. Internally, the part is emitter functional logic (EFL), similar in design to ECL.

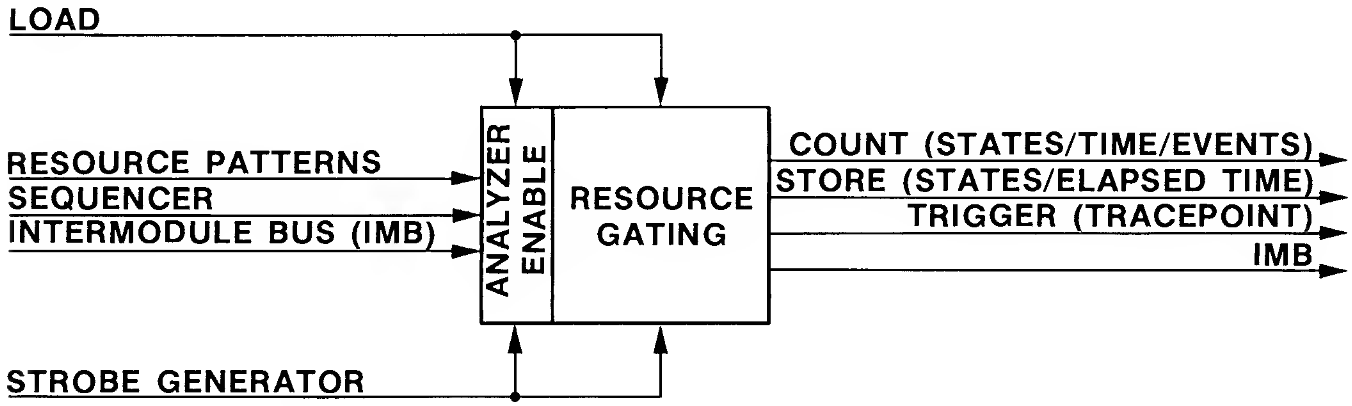


Figure 8-8. Analysis Controller Summary

8-99. Modes.

8-100. The Analysis Controller has two primary modes, run mode and load mode, controlled by LRUN and LLD. The load mode is used to program a 58 bit shift register inside the Analysis Controller. The parallel outputs of the register initialize and determine which of the various inputs will control the Analysis Controller during a trace execution. The 58 bits are grouped as follows:

Storage Function	3 bits
Trigger Function	6 bits
Master Enable Function	4 bits
Resource Pattern Allocation	30 bits
Initialize Poststore	10 bits
Initialize Sequencer Enables	5 bits

The run mode is used while executing a trace.

8-101. Two secondary modes are used during performance verification: run_load mode with both LRUN and LLD low, and not run_not load mode with both LRUN and LLD high. Run_load mode allows the Analysis Controller to run but excludes external clocks. Not run _not load mode is used while testing the Sequencer.

8-102. Block Diagram.

8-103. The Block Diagram shows a time progression from the arrival of resource patterns to output of control signals including write control. First there is Resource Allocation, then Resource Gating, then Write Qualification. Additional major sub-blocks include Analyzer Enable, and IMB Receive and Drive.

8-104. The 58 bit shift register selects which of these sub-blocks or inputs will actively be used to produce an output. Finally, the Sequencer plays a major role in controlling the State Analysis Subsystem and is referenced in the Block Diagram even though it is not physically part of the Analysis Controller.

8-105. Resource Allocation. On the Acquisition Boards, trace data addresses the Resource Pattern Trigger Memories, and the Memories output an 8 bit pattern (wire ORed accross all boards) which forms the Resource Pattern input (LBRP0-7) for the Analysis Controller. Inside the Analysis Controller, these eight signals are allocated to various functions, with the following limitations: the sum of the resources cannot exceed eight; trigger and store can use up to eight resources; count can use up to four resources (LBRP2,3,6,7); overview count can use up to four resources (LBRP0,1,4,5); four resources can be ranges provided a 20 channel board is present; a "not" condition requires two resources. The 58 bit shift register uses 30 bits to specify which terms will be used by which function. The following table shows an example for resource allocation:

STATE RECOGNITION RESOURCES

```
trigger on ADDRESS = 4000H and STATUS = Mem_read        #1
        or ADDRESS = 4000H and DATA <> 0             #2,#3
        or ADDRESS = range 0H thru 0FFH                 #4

  store on ADDRESS = range 4000H thru 4135H             #5
        or ADDRESS = 0F000H                             #6

  count on ADDRESS = 6000H                              #7
        or  STATUS = IO_in                              #8
```

8-106. The table shows 4 resources used by trigger, 2 by store and 2 by count. Because of the "DATA <> 0", the second specification line for trigger required 2 resources. Internally, this is done by DME (disjoint minterm event) gating, which requires one resource to find DATA = 0, and a second resource to invert it. Pipeline Strobe (HPLS) latches the count, store and trigger resources, and they are applied to Resource Gating.

8-107. Resource Gating. The count, storage and trigger resources are gated with the Sequencer, IMB, and Analyzer Enable, and output as Overview Count Qualify (HOCQ), Store Flag (LSFLG) and Trigger (NTR). The 58 bit shift register uses 18 bits (Storage Function, Trigger Function, Analyzer Enable Function, Initialize Sequencer enables) to specify which inputs to Resource Gating will be looked at. The default state for these bits cause the Analysis Controller to count everything, store always, and trigger on anything.

8-108. Write Qualification. Write Qualify Gating determines which trace data will be written into the Trace Pod Data Memories. Low Strobe Enable (LSE) is directly produced by Storage Qualify Gating, and can be modified by the Trace Point Latch and the Measurement Complete Latch. The Trace Point Latch is set by the first trigger (NTR), then it enables the Post-Trace Point Counter to count each time data is

stored in the Trace Memories. The Post-Trace Point Counter counts the number of states to be stored after trace point, then sets the Measurement Complete (NMC) Latch, which disables the Write Qualify Gating (forces HWQ to go low). The 58 bit shift register uses 10 bits (Initialize Poststore) to initialize the two latches and the PostTrace Point Counter.

NOTE

> Writing to the Overview Event Memory is not controlled by the Write Qualification function. Overview writing is controlled directly by the Sequencer and Analyzer Enable.

8-109. NTR produces a pulse each time the trigger event occurs, and can be used to trigger external test equipment. NMC can be routed to external test equipment, and also serve as an overflow for the 58 bit shift register. The overflow function is used during performance verification to test the loading of the Analysis Controller. Data is input on bit 0 of the data bus (LDB0) and clocked by Positive Write Analysis Controller (PWAC). Low Load (LLD) must be low to clock in data.

8-110. **Analyzer Enable.** This is the master enable for the entire State Analyzer. Master Enable (LME) can be set low by Run (LRUN) which is a keyboard command to begin execution, or it can be received from the IMB. When LME is strobed by State Recognition Strobe (HSRS), it latches Analyzer Enable 1 (HAE1). When HAE1 is strobed by Pipeline Strobe (HPLS), it produces Positive Pipeline Strobe (PPLS) which is used to strobe the Sequencer, the Data Pipeline Registers, and Analyzer Enable 2 (HAE2). When HAE2 is strobed by Write (HWRT), it produces High Bus Overview Write Strobe (HBOWRT) and Positive Sequence Occurence Counter Increment (PSOCINC). HBOWRT is used to write to the Overview Event Memories on the 20 Channel Acquisition Board.

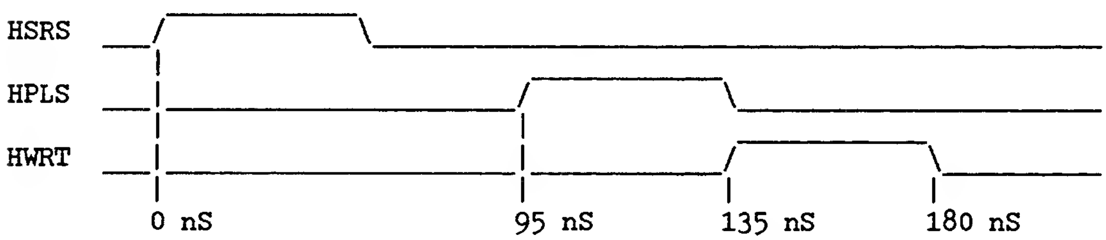
8-111. Another source of master enable is the Sequencer. When the Sequencer finds all of the required states in the order specified, it can drive Sequence Master Enable (LSME) low. LSME then enables the trigger and store functions in the Analysis Controller. LSME can also be programmed to drive LME on the IMB. The 58 bit shift register uses 4 bits to specify whether or not the IMB or Sequencer will control Master Enable.

8-112. **IMB Receive and Drive.** Master Enable, Trigger and Store functions can be received by the Analysis Controller from the IMB. The Analysis Controller can transmit (drive) Delayed Clock (PDC), as well as Master Enable (LME), Trigger (HTR), Trigger Enable (LTE), and Store Enable (LSE). When the Analysis Controller is receiving IMB signals, the signals are latched with the State Recognition Strobe (HSRS) and applied to the Resource Gating after Pipeline Strobe (HPLS). When the Analysis Controller is driving the IMB, they are strobed out by Write (HWRT). The 58 bit shift register is responsible for determining which IMB signals are active.

8-113. **Sequencer.** The Sequencer is an integral part of the Control Board and should be considered an extension of the Analysis Controller. The inputs to the Resource Gating from the Sequencer are similar to the inputs from the IMB Receiver. It is the 58 bit shift register which determines which circuitry will actively control the State Analyzer during a particular run. The Sequencer can perform a master enable function by setting Sequence Master Enable (LSME) low. The Sequencer alone controls Overview Enable (LOVEN) and Overview Reset (LOVRST).

8-114. Timing of Analysis Controller.

8-115. The Strobe Generator controls timing of the Analysis Controller by use of State Recognition Strobe (HSRS), Pipeline Strobe (HPLS) and Write Strobe (HWRT).



Prior to Resource Allocation, the Resource Patterns, Analyzer Enable, and IMB are clocked by HSRS. After Resource Allocation, HPLS clocks the Sequencer and all other inputs, so that Resource Gating is valid. Finally, HWRT clocks out write signals, and HWRT going low clocks the IMB Drive. Internal delays are in the several nanosecond range due to the EFL logic design.

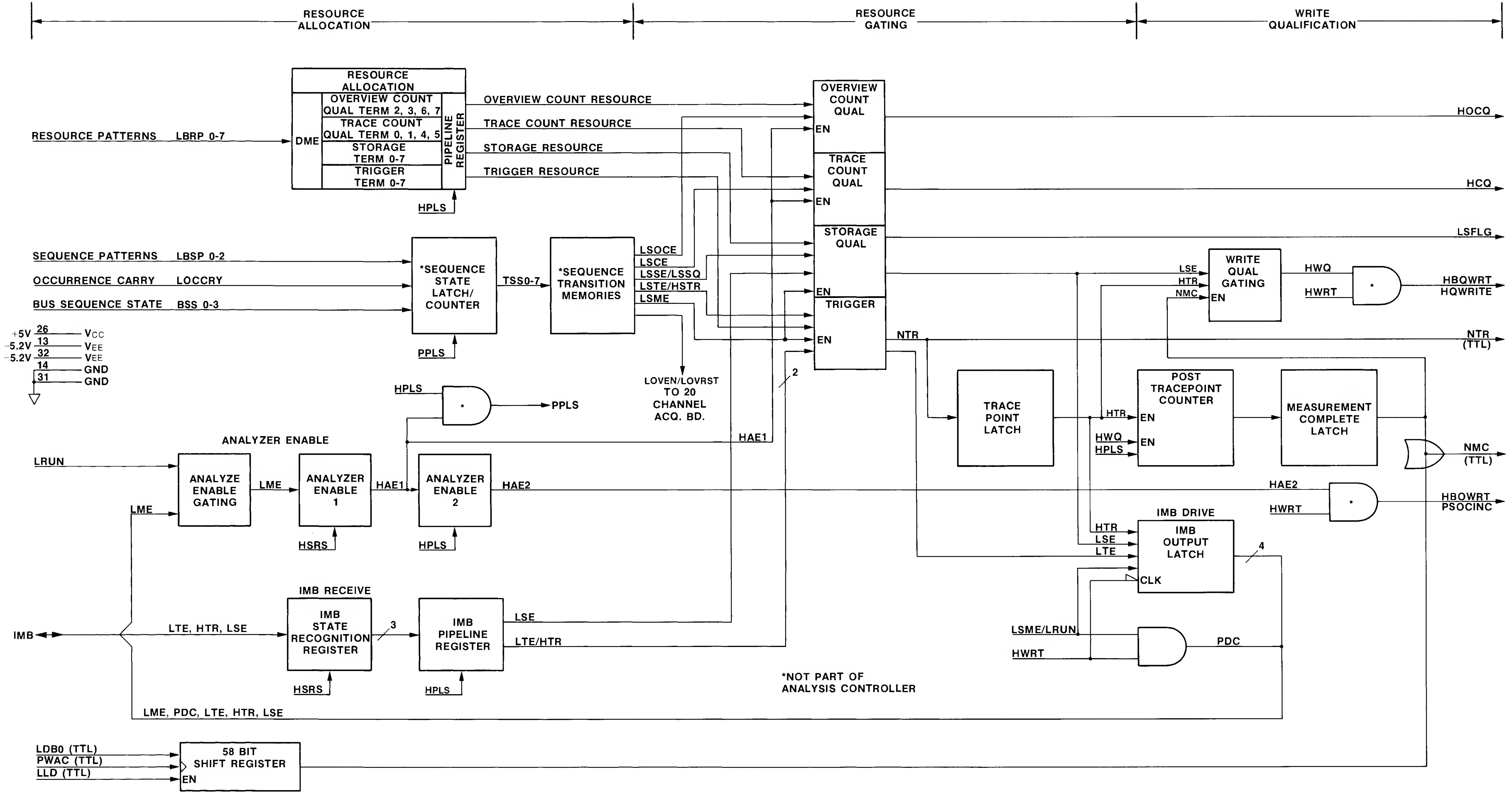


Figure 8-9.
Analysis Controller Block Diagram

8-116. STATE/TIME COUNTER.

8-117. Description.

8-118. The State/Time Counter is a custom designed 20 bit Gray Code counter with prescale. The prescaler allows it to count up to 750,000,000,000 states in the count states mode, and 8+ hours at a 25 MHz rate in the count time mode. Externally, the Counter is ECL except for three TTL inputs. Internally, it is emitter-functional- logic (EFL). Chip delay from clock edge to counter outputs is approximately 25 nS without prescale. With prescale, chip delay can exceed 100 nS. There are 5 prescale factors: 1. divide by 1, 2. divide by 8, 3. divide by 2 e10, 4. divide by 2 e17, and 5. divide by 2 e24.

8-119. Where Used.

8-120. The counter is used on both the 64621A Control Board and the 64623A 20 Channel Acquisition Board.

8-121. On the Control Board, the Counter is used during trace (256 states), and is used during Overview on the 20 Channel Board. Pin 35 controls the Trace/Overview modes. On the Control Board pin 35 is tied low, the Trace mode. On the 20 Channel Board pin 35 is tied high for the Overview mode.

8-122. LSTATE, pin 8, makes the decision to count either qualified states or time intervals. When LSTATE is low, states between stored qualified states will be counted. When LSTATE is high, time between stored qualified states will be counted.

8-123. Function.

8-124. **Modes.** The counter has two modes, the load mode and the normal mode. The load mode is used during Performance Verification. It forces the Counter to act like two ten-bit counters without prescale, which qreatly improves loading and testing efficiency. The normal mode is described in the Block Diagram description.

8-125. **Block diagram.** The Block Diagram shows inputs on the left and outputs on the right. The three major sections are counter control, 20 bit counter, and the output latch.

8-126. **Counter Control.** The counter control section controls the count, reset, and latch functions. The counter's versatility is shown by the triple 2 to 4 selector, one selector for each function. Using the count function as an example, if pin 8 is a logic high and pin 35 is a logic high, then overview on time is selected, which is input 3 to all functions of the selector. This means that the control section will count using 25 MHz as input (PINC is used to count states); it will reset when PSET goes high, and it will latch the count when PLATCH goes high. The count pulse must be enabled by a high counter enable (HCE) in order to reach the prescale circuitry. The prescaler will pass pulses directly to the 20 bit counter until the count exceeds 611,000. Then the 3 bit exponent will cause the prescaler to divide by 8 before allowing a count pulse. As the count increases, the prescaler will divide by 2 e10, 2 e17 and finally 2 e24.

8-127. **PSET (Positive Set).** PSET is an edge sensitive input which resets the counter to a known state. The counter is locked in that state until the reset function is clocked by 25 MHz. The half -way AND gate does not allow PSET to reset the counter until it has counted to at least half-way through the divide-by-1 range.

8-128. 20 Bit Counter. The counter provides a 20 bit output consisting of 3 bit exponent and a 17 bit mantissa. It operates either as a time counter or as a state counter. The time count mode provides a minimum resolution of 40 nS with a minimum 3 digit accuracy from 100 nS to 30 kS (8 hours). The state count mode provides single state resolution to 611,670 states, and prescaled counts up to 750,000,000,000 states. Because it counts in Gray Code (only one bit changes for each new state), the outputs appear to change without a pattern. The counter outputs are reset after each storage event (an exception is > halfway restriction in time count), which produces a relative count.

8-129. Output Latch. The Output Latch is controlled by a gate and an output enable. When PLATCH goes high, the counter outputs are latched. The exception is PSET. When PSET is low and trace state is selected, the latch is transparent; when PSET goes high, the counter outputs are latched. Low output enable (LOE) enables the output drivers. The counter outputs will be low when LOE is high, or when the counter is reset, latched and LOE goes low.

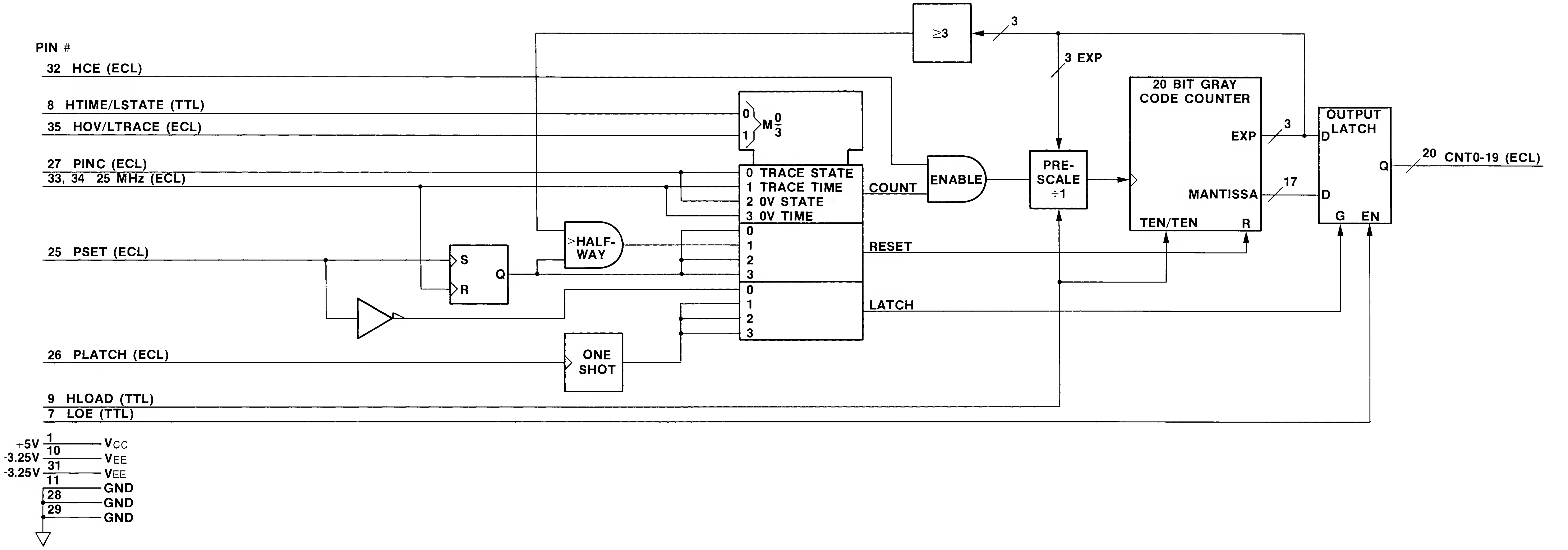


Figure 8-10.
State/Time Counter Block Diagram
SAC 8-26

8-130. MNEMONICS.

8-131. The signals in this product have been assigned mnemonics that indicate the true state, and the function of the signal line. In general the first character indicates the true state, H for high, l for low. If the signal is used with an edge sensitive device, P for positive, and N for negative is used to indicate the edge that the signal becomes true on. No indication of the voltage levels is given, i.e., TTL, ECL, MOS. This information is given on the schematic using the newer type of Logic Symbology.

Table 8-1. Mnemonics

Mnemonic	Description
BSS0-3	Bus Sequence State 0-3 --a feed back path within the Sequencer that enables it to change from one state to the next. A state may require that an event occur only once, or it may require the event to occur many times before changing to the next state.
CD0-7	Counter Data 0-7 -- outputs of the Trace Counter/Status Memories. The information stored in the Memories represents the time between two stored states, or the number of states between two stored states. A value for each measurement is stored and returned to the CPU (CD0-7, LDB0-7) over the CPU's Data Bus for formatting and display on the CRT. The sequence state for each measurement is also returned to the CPU by CD0-7.
CNT0-19	Count 0-19 --outputs of the Trace State/Time Counter. CNT0-19 represents the time between two stored states, or the number of states between two stored states. The value (CNT0-19) for each measurement is stored in the Trace Count/Status Memory.
GNDSEN	Ground Sense -- the return path from the Clock Probe for the Clock Threshold Digital to Analog Converters.
HBOTF	High Bus Overview Trigger Flag -- from the ACQ Board. When high, indicates that the 20 Channel Acquisition Board has seen a qualified trigger event. (A trigger event is a single occurrence of an event decoded from input data or from the Overview State/Time Counter.) HBOTF comes from the 20 Channel ACQ Board only.
HBOVCQ	High Bus Overview Count Qualify -- sent only to the 20 Channel Data Acquisition Board. When high, HBOVCQ allows the Overview Counter to increment. HBOVCQ may be driven by the Analysis Controller or HOVCQ.
HBOWRT	High Bus Overview Write -- sent to the 20 Channel Acquisition Board only. When high, HBOWRT enables write circuits on the 20 Channel ACQ Board for writing to the Overview Event Memories. HBOWRT is also used to increment the Overview Trace State/Time Counter, and can drive PSOCINC due to a wire OR connection (see PSOCINC). When enabled on the 20 Channel Data Acquisition Board, HBOWRT allows the Overview Event Memories to be written to and increments the Overview Memory Address Counters.
HBQWRT	High Bus Qualified Write -- when high, HBQWRT synchronizes the Trace Pod Data Memories in the Acquisition Boards with the Trace Counter/Status

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
	Memories in the Control Board. When low, HBQWRT increments the Trace Pod Data Memory Address Counters in the Data Acquisition Boards. HBQWRT is enabled by HWQ, and is derived from HWRT.
HCD0-1	High Clock Data 0-1 -- outputs from the Clock Term Generator, U25, returned to the Mainframe. Used in Performance Verification to indicate that the Term Generator can respond to the various combinations of clocks and qualifiers input from the Clock Probe or Preprocessor.
HCLK0-7	High Clock 0-7 -- differential (LCLK0-7) clock signals or qualifier bits from the user's equipment. The eight bits are defined to be clocks or qualifiers by keyboard entry. HCLK0-7 may come from either the Clock Probe or the Preprocessor.
HCQ	High Count Qualify -- when high, HCQ enables the Trace State/Time Counter to increment. HCQ develops HCQB. The status of HCQ is stored in the Trace Count/Status Memory. When a high is stored for HCQ, the software will add the value one to the stored value in the Trace Count/Status Memory.
HCQB	High Count Qualify Buffered -- a flag returned to the CPU. When high, HCQB indicates that the Trace State/Time Counter may have been counting when the user's information was stored.
HCTST	High Count Test -- used when testing the Trace State/Time Counter. When high, HCTST divides the Counter into two ten bit counters. HCTST is controlled by the CPU.
HDVLD	High Data Valid -- derived from the Strobe Generator. When high, HDVLD has latched CD0-7 into the Trace Data Read Register. When LRTDR is low, the latched information is presented to the CPU over the Data Bus. HDVLD is also returned to the CPU through the Analysis Status Buffer indicating that information has been latched into the Trace Data Read Register.
HENHLT	High Enable Halt -- when high, HENHLT allows PHALT to be sent to the Preprocessor. HENHLT is CPU controlled.
HENSTIM	High Enable Stimulus -- when high, HENSTIM allows PSTIM to be sent to the Preprocessor. HENSTIM is CPU controlled.
HINV	High Invert -- when high, inverts the two signals going to PORT1 and PORT2. The inversion may be selected by a keyboard command.
HLD	High Load -- when high, HLD switches the Sequence State Latches/Counter to the count mode. The outputs of the Counter are used to address the Sequence Transition Memories while loading information from the CPU (LDB0-7/LSEQD0-7). HLD and LLD are asserted at the same time.
HMCLK	High Master Clock -- when going from a low to a high, HMCLK indicates that the eight clock inputs have satisfied the requirements that have been programmed into the Clock Term Generator by the CPU and has started the Strobe Generator Cycle. HMCLK is wire ORed with PPVSTB and PBSTBRQ.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
HOTFB	High Overview Trigger Flag Buffered -- from the ACQ Board. When high, indicates that the 20 Channel Acquisition Board has seen a qualified trigger event. (A trigger event is a single occurrence of an event decoded from input data or from the Overview State/Time Counter.) HOTFB comes from the 20 Channel ACQ Board only.
HOVCQ	High Overview Count Qualify -- HOVCQ becomes HBOVCQ. When high, HOVCQ allows the Overview Counter on the 20 Channel Data Acquisition Board to increment. HOVCQ is derived from the Analysis Controller or HLD.
HOVS	High Overview Strobe -- generated in the Strobe Generator. Develops LBOVEN and PBOVRST. These two signals are used on the 20 Channel Data Acquisition Board only.
HPLS	High Pipeline Strobe -- developed in the Strobe Generator. HPLS is used by the Control Board and both Data Acquisition Boards for latching information into the Pipeline Reqisters at the correct time in the Analyzer's timing cycle (PBPLS).
HQWRITE	High Qualified Write --when high, HQWRITE is used to write to the Trace Counter/Status Memories, and to internally reset the Trace State/Time Counter. HQWRITE going low increments the Trace Count/Status Memory Address Counter. HQWRITE is derived from HWRT and enabled by HWQ.
HSRS	High State Recognition Strobe -- developed in the Strobe Generator. HSRS is used to clock the State Recognition Register in the Analysis Control chip. The purpose of the register is to store information received on the Intermodule Bus (IMB). HSRS also clocks LRUN.
HSTR	High Sequence Trigger -- when high, indicates that a Sequence Trigger has been found.
HTCLK	High Transfer Clock -- a differential clock (LTCLK) used in the Preprocessor. When HTCLK goes from a low state to a high state, data is transferred to/from the State Analyzer and the Preprocessor.
HTIMS	High Time Strobe -- developed in the Strobe Generator. Used in the Trace State/Time Counter (PLATCH). When HTIMS goes from a low to a high, the information inside the Trace State/Time Counter is latched into its output latches.
HTR	High Trigger -- HTR is one of the bidirectional signals that make up the Intermodule Bus (IMB). HTR is used to indicate to other modules connected to the IMB that a trigger event has been found. Being bidirectional, the State Analyzer can tell other modules that it has found a trigger, or observe that another module has found a trigger event. HTR is wire ORed with other modules.
HWQ	High Write Qualify -- generated by the Analysis Controller. HWQ is used to enable HBQWRT, and stops the Trace State/Time Counter when the output of the Counter is being stored in the Trace Counter/Status Memories.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
HWRT	High Write -- developed in the Strobe Generator. HWRT is used to transfer storage commands from the inputs to the outputs of the Analysis Controller at the correct time in the data acquisition cycle, and to provide timing for other write signals.
L25MHZ	Low 25 Megahertz -- a high accuracy crystal controlled clock originating in the Mainframe. L25MHZ is used to clock the Trace State/Time Counter when in the time mode for measuring time between states.
LA0-13	Low Address 0-13 -- a 16 bit address bus generated by the CPU and used to address various devices in the system. Only bits 0-13 are used in this model.
LAB0-13	Low Address Buffered 0-13 -- same as LA0-13 with additional buffering. LAB0-13 may also be latched from the Address Bus.
LBCLR	Low Bus Clear -- same as LCLR except buffered. LBCLR is sent to the 20 and 40 Channel Data Acquisition Boards to clear various counters and registers.
LBMACS	Low Bus Memory Address Counter Select -- developed in the Strobe Generator. Used in the 20 and 40 Channel Data Acquisition Boards. When low LBMACS allows the Memory Address Counters (on the ACQ Boards) to address the Trace Pod Data Memories. When high, the CPU can address the Memories over the CPU Address Bus.
LBOVEN	Low Bus Overview Enable -- developed from HOVS. LBOVEN is used only on the 20 Channel Data Acquisition Board. When low, LBOVEN allows the Overview section to look for its trigger events and enables overview storage.
LBRP0-7	Low Bus Resource Pattern 0-7 -- eight signals coming from the Data Acquisition Boards. When low, indicates to the Analysis Controller that combinations of Trigger, Storage, and Count information have been detected.
LBSP0-3	Low Bus Sequence Pattern 0-3 -- four signals coming from the Data Acquisition Boards. When low, they indicate to the Sequencer that the Data Acquisition Boards have found the Sequence State(s) requested by the user.
LCLK0-7	Low Clock 0-7 -- differential (HCLK0-7) clock signals or qualifier bits from the user's equipment. The eight bits are defined to be clocks or qualifiers by keyboard entry. LCLK0-7 may come from either the Clock Probe or the Preprocessor.
LCLR	Low Clear -- used to clear various counters and registers on the Control Board. Derived from the CPU Address Bus and other Mainframe control lines. LCLR is also used on the 20 and 40 Channel Data Acquisition Boards (LBCLR) to clear various counters and registers.
LD0-12	Low Data 0-12 -- a 16 bit bidirectional bus used to transfer data to and from the CPU. When LSTB is low, the data on the bus is valid. Only bits 0-12 are used in this model.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LDB0-7	Low Data Buffered 0-7 -- same as LD0-7 with additional buffering. LDB0-7 is distributed throughout the State Analyzer Control Board.
LDV	Low Data Valid -- developed by the Strobe Generator. When low, LDV indicates that the Trace Memory outputs are stable and the CPU may read them.
LDVTTL	Low Data Valid TTL -- LDVTTL is used to clock the Trace Point Register. LDVTTL is derived from LDV in the Strobe Generator.
LIA0-3	Low Interface Address 0-3 -- signals used for reading and writing information in the Preprocessor. LIA0-3 are derived from the CPU's Address Bus.
LID	Low Identification -- a signal originating in the Mainframe. When low, the CPU is requesting that the Board Identification be sent from the State Analyzer Control Board to the CPU over the Data Bus on data bits 8 and 12.
LIDB	Low Identification Buffered -- a signal originating in the Mainframe and buffered on the State Analyzer Control Board. See LID.
LID0-7	Low Interface Data 0-7 -- a bidirectional data bus between the Preprocessor and the Control Board. LID0-7 are derived from the CPU's bidirectional Data Bus.
LIWRT	Low Interface Write -- one of the control lines from the Control Board to the Preprocessor. When low, the Control Board is writing to the addressed device, i.e., the Preprocessor. LIWRT is the same as LWRT except buffered two times (LWRTB).
LLD	Low Load -- when low, LLD allows the internal registers of the Analysis Controller to be loaded with serial data (LBD0) from the CPU. LLD and HLD are asserted at the same time.
LMACS	Low Memory Address Counter Select -- developed in the Strobe Generator. When low, LMACS allows the Trace Count/Status Memory Address Counters (on the Control Board) to address the Trace Counter/Status Memories. When high, the CPU can address the Memories over the CPU Address Bus.
LMAP2	Low Map 2 -- a signal developed by the CPU. LMAP2 is used as the Start/Stop Pulse in Signature Analysis and appears only on the extender card.
LMC	Low Measurement Complete -- when low, LMC indicates that the State Analyzer has stored all the information requested by the user in the Trace Memories.
LME	Low Measurement Enable -- LME is one of the bidirectional signals that make up the Intermodule Bus (IMB). When LME is low, the State Analyzer is allowed to operate in a normal mode without waiting for other modules. If the State Analyzer is operating in the Measurement Enable Mode and LME is high, it may not drive or receive any IMB functions. LME is wire ORed with other modules.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LMS	Low Memory Select -- developed from LSEL and LSTM. When low, LMS latches the CPU Address Bus (LA0-13), LWRT, and LID into the Address Latches. At the same time, LMS enables the CPU Data Buffer (bidirectional). If LRSTB is low, the CPU can send information to the Control Board over the CPU Data Bus (LD0-12). If LRSTB is high, the CPU can read information from the Control Board.
LMSYN	Low Memory Synchronize -- a signal sent to the CPU. When low, the CPU is forced to wait until the Control Board can complete a read or write operation.
LMV	Low Memory Valid -- developed by the Strobe Generator. When low, LMV generates PMACRS and NMACRS if PBRSTB has occurred.
LOCCRY	Low Occurrence Carry -- when low, LOCCRY indicates that the Sequence Occurrence Counters have reached terminal count.
LOVEN	Low Overview Enable -- LOVEN is sent only to the 20 Channel Data Acquisition Board. When low, LOVEN allows the Overview section to look for its Trigger Events. LOVEN is strobed to the 20 Channel Board with HOVS. LOVEN is developed in the Sequencer.
LOVRST	Low Overview Reset -- developed in the Sequencer and used only in the 20 Channel Data Acquisition Board. LOVRST is used to reset the Overview Counter.
LPOP	Low Power On Preset -- when low (during Mainframe power-up or during A.C. power line disturbances), LPOP resets various latches, counters, and registers to a known state. When LPOP returns to a high state, the Mainframe begins executing software.
LPPBEN	Low Preprocessor Buffer Enable -- when low, LPPBEN enables the Preprocessor Data and Address Buffers to allow information to be transferred to/from the Preprocessor.
LPPSTB	Low Preprocessor Strobe -- developed in the Mainframe Interface Circuits. LPPSTB develops HTCLK/LTCLK. LPPSTB transfers data to/from the State Analyzer and the Preprocessor.
LRC	Low Register Clock -- a clock developed from the CPU's Address Bus and LWRT. LRC is used to latch information from the CPU's Data Bus into Control Registers U120 and U123, generating various control signals for the State Analyzer Control Board.
LRDEN	Low Read Enable -- developed in the Mainframe Interface Address Decoder. When low, LRDEN enables the CPU Read Decoder. The CPU Read Decoder in turn selects one of five registers or buffers to place information from the Control Board onto the CPU Data Bus.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LRMACR	Low Read Memory Address Counter Register -- when low, LRMAC enables the Trace Memory Address Counter Read Register allowing the value of the Trace Count/Status Memory Address Counters to be read over the CPU's Data Bus.
LRSQRG	Low Read Sequence Register -- when low, LRSQRG enables the Sequence Read Register allowing the value of the Sequence State Latch/Counters (TSS0-7) to be read over the CPU's Data Bus.
LRSTB	Low Read Strobe -- developed in the Mainframe Interface from LWRTB and LIDB, LSTB and LSEL. When low, LRSTB allows information to be placed on the CPU Data Bus.
LRSTS	Low Read Status -- when low, LRSTS enables the Analysis Status Buffer allowing the states of eight different signals to be read over the CPU's Data Bus.
LRSTSS	Low Reset Sequence State Counter -- when low, LRSTSS resets the Sequence State Counter to zero. The Counters cannot begin counting until LRSTSS returns to a high state. LRSTSS is developed from the CPU's Address Bus and other control lines from the CPU.
LRTDR	Low Read Trace Data Register -- when low, LRTDR enables the Trace Data Read Register allowing the contents of the Trace Counter/Status Memories (CD0-7) to be read over the CPU's Data Bus.
LRTPRG	Low Read Trace Point Register -- when low, LRTPRG enables the Trace Point Register allowing the value of the Trace Count/Status Memory Address Counters to be read over the CPU's Data Bus.
LRUN	Low Run -- master enable for the Control Board generated by the CPU. When low, LRUN enables the Analysis Controller and is returned to the CPU through the Analysis Status Buffer.
LSCE	Low Sequence Counter Enable -- a Sequencer output used by the Analysis Controller to determine when the Trace State/Time Counter should be enabled.
LSCLK	Low Slow Clock -- when low, LSCLK indicates that it has been at least 100 mS since the last HMCLK. The status of LSCLK is returned to the CPU through the Analysis Status Buffer over the CPU Data Bus.
LSE	Low Storage Enable -- LSE is one of the bidirectional signals that make up the Intermodule Bus (IMB). When LSE is low, the Storage Qualify function is enabled in the State Analyzer and will store information when another module tells it to. LSE is wire ORed with other modules.
LSEL	Low Select -- a signal originating in the Mainframe. When low, LSEL allows the State Analyzer Identification Code to be returned over the CPU's Data Bus. This allows the CPU to identify if there is a State Analyzer Control Board installed in the Mainframe, and if so which slot of the Card Cage it

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
	is installed in. LSEL is also used to enable the State Analyzer Control Board.
LSEQD0-7	Low Sequence Data 0-7 -- the data path the CPU uses to load information into the Sequence Transition and Sequence Occurrence Memories prior to a measurement (LD0-7, LDB0-7, and LSEQD0-7).
LSFLG	Low Store Flag -- an Analysis Controller output. LSFLG is used as a flag in the Trace Counter/Status Memories. When low, LSFLG indicates when storage is enabled.
LSFLGB	Low Store Flag Buffered -- LSFLGB is the same as LSFLG except translated from an ECL level to a TTL level. When low, LSFLG indicates when storage is enabled.
LSME	Low Sequence Master Enable -- an Analysis Controller input. When low, LSME enables the LRUN portion of the Analysis Controller. LSME is an output of the Sequence Transition Memory.
LSOCE	Low Sequence Overview Count Enable -- an Analysis Controller input. When low, LSOCE enables LBRP0-7 to generate HOVCQ. LSOCE is an output of the Sequence Transition Memory.
LSOCEN	Low Sequence Occurrence Counter Enable -- when low, LSOCEN allows the Sequence Occurrence Counters to count up. The command to enable is stored in the Sequencer by the CPU (LDB0-7, LSEQD0-7). LSOCEN is an output of the Sequence Transition Memory.
LSOCLD	Low Sequence Occurrence Counter Load -- when low, LSOCLD allows the value stored in the Sequence Occurrence Memories to be loaded into the Sequence Occurrence Counters. The command to load the Counters is stored in the Sequencer by the CPU (LDB0-7, LSEQD0-7). LSOCLD is an output of the Sequence Transition Memory.
LSSE	Low Sequence Store Enable -- an Analysis Controller input. When low, LSSE enables LBR0-7 to generate LSFLG. LSSE also enables HWQ. LSSE is and output of the Sequence Transition Memory.
LSSQ	Low Sequence Store Qualify -- an Analysis Controller input. When low, LSSQ qualifies LBRP0-7. When qualified, LBRP0-7 generates LSFLG. LSSQ also qualifies HWQ. LSSQ is an output of the Sequence Transition Memory.
LSTATE	Low State -- LSTATE controls the two modes of the Trace State /Time Counter. When LSTATE is low, the Counter counts the number of states between two stored states. PINC is used to increment the counter in the state mode. When LSTATE is high, the Counter counts time using L25MHZ as a reference.
LSTB	Low Strobe -- a signal orginating in the Mainframe. When low and the CPU is in the write mode (LWRT low), LSTB indicates the Data Bus has valid

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
	information on it. When low and in the read mode, LSTB indicates that the CPU is not driving the Data Bus, and the device addressed may now drive it.
LSTE	Low Sequence Trigger Enable -- a Sequencer output used by the Analysis Controller. When LSTE is low, the Analysis Controller enables NTRIG.
LSTM	Low Start Memory -- a signal originating in the Mainframe. When low, LSTM indicates that the information on the CPU's Address Bus is valid.
LTCLK	Low Transfer Clock -- a differential clock (HTCLK) used in the Preprocessor. When LTCLK goes from a high state to a low state, data is transferred between the State Analyzer and the Preprocessor.
LTCSMS0-3	Low Trace Count/Status Memory Select 0-3 -- LTCSMS is used to enable (chip select) the Trace Counter/Status Memories.
LTE	Low Trigger Enable -- LTE is one of the bidirectional signals that make up the Intermodule Bus (IMB). When LTE is low, the Trigger Recognition function is enabled in the State Analyzer. LTE is wire ORed with other modules.
LTP	Low Trace Point -- LTP is normally high. The transition from high to low indicates that the State Analyzer has found the Trigger Event requested by the user.
LTRCP	Low Trace Point -- LTRCP is normally high. The transition from high to low indicates that the State Analyzer has found the Trigger Event requested by the user. LTRCP is returned to the CPU through the Analysis Status Buffer.
LWOCML	Low Write Occurrence Memory Lower -- when low, the CPU can load information into the Lower Sequence Occurrence Memories (LSEQD0-7).
LWOCMU	Low Write Occurrence Memory Upper -- when low, the CPU can load information into the Upper Sequence Occurrence Memories (LSEQD0-7).
LWRAP	Low Wrap -- a status signal returned to the CPU at the CPU's request. When low, LWRAP indicates that the Trace Counter/Status Memories are full of information.
LWRT	Low Write -- one of the control lines from the Mainframe. When low, the CPU is writing to the addressed device, i.e., the State Analyzer Control Board.
LWRTB	Low Write Buffered -- one of the control lines from the Mainframe with additional buffering. When low, the CPU is writing to the addressed device, i.e., the State Analyzer Control Board.
LWRTSTB	Low Write Strobe -- CPU controlled. When low, LWRTSTB enables the Mainframe Interface Write Decoders when the CPU wants to do a write cycle on the Control Board.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LWSEQML	Low Write Sequence Memory Lower -- when low, the CPU can load information into the Lower Sequence Transition Memories (LSEQD0-7). LWSEQML is developed in the Write Decoders.
LWSEQMU	Low Write Sequence Memory Upper -- when low, the CPU can load information into the Upper Sequence Transition Memories (LSEQD0-7). LWSEQMU is developed in the Write Decoders.
LWTHS1	Low Write Threshold 1 -- when LWTHS1 goes from a high to a low, information from the CPU is latched into the Digital to Analog Converter. The output current is proportional to the binary value latched. ((Full Scale Current X Binary Value Latched)/256 = Output Current.)
LWTHS2	Low Write Threshold 2 -- when LWTHS2 goes from a high to a low, information from the CPU is latched into the Digital to Analog Converter. The output current is proportional to the binary value latched. ((Full Scale Current X Binary Value Latched)/256 = Output Current.)
NBDSTB	Negative Bus Data Strobe -- a differential signal (PBDSTB), developed in the Strobe Generator. Used to latch the outputs of the Trace Pod Data Memories into the Trace Pod Data Latch on the Data Acquisition Boards.
NBSRS	Negative Bus State Recognition Strobe -- a differential strobe (PBSRS) developed in the Strobe Generator, and sent to the Data Acquisition Boards. At the beginning of a data acquisition cycle, NBSRS goes from a high state to a low state. NBSRS is used to latch user information into the State Recognition Latches/Counters.
NDSTB	Negative Data Strobe -- a differential signal (PDSTB) developed in the Strobe Generator. NDSTB and PDSTB are used to develop HDVLD (see HDVLD).
NIHALT	Negative Interface Halt -- a differential signal (PIHALT) sent to the Preprocessor that can be used to halt the user's system.
NINCSS	Negative Increment Sequence State -- when NINCSS goes from a high to a low state, the Sequence State Latch/Counter will be incremented one state when in the count mode. NINCSS is developed by the CPU and is wire ORed with PPLS.
NISTIM	Negative Interface Stimulus -- a differential signal (PISTIM) sent to the Preprocessor. NISTIM is developed from PSTIM when enabled by HENSTIM. NISTIM goes from a high to a low state when a Trigger Event or Sequence Event occurs if enabled by the user.
NMACRS	Negative Memory Address Counter Register Strobe -- a differential signal (PMACRS) developed in the Strobe Generator. NMACRS is used to latch information from the Trace Count/Status Memory Address Counters into the Trace Memory Address Counter Read Register. The information in the Register is placed on the CPU Data Bus when LRMACR goes low.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
NMC	Negative Measurement Complete -- an output from the Analysis Controller. When low, NMC indicates to the CPU that the information requested by the user has been stored in the Trace Memories. NMC also latches LMC into the Port Latch.
NOCSTB	Negative Occurrence Counter Strobe -- NOCSTB is developed from the CPU's Address Bus and other control lines from the CPU. NOCSTB is used to develop PSOCINC. NOCSTB is used only during performance verification.
NSEQEV	Negative Sequence Event -- when going from a high state to a low state, NSEQEV indicates that either a Sequence Event has been found, or the Sequence Occurrence Counters have been incremented. NSEQEV can develop PSTIM, a State Analyzer output.
NSQRGS	Negative Sequence Register Strobe -- a differential signal (PSQRGS) developed in the Strobe Generator. NSQRGS is used to latch information from the Sequence State Latch/Counters into the Sequence Read Register. The information in the Register is placed on the CPU Data Bus when LRSQRG goes low.
NTRIG	Negative Trigger -- an Analysis Controller output. NTRIG goes from a high state to a low state each time the Trigger Event specified by the user occurs. NTRIG latches LTP into the Port Latch and LTRCP into the Trace Point Latch.
PBDSTB	Positive Bus Data Strobe -- a differential signal (NBDSTB), developed in the Strobe Generator. Used to latch the outputs of the Trace Pod Data Memories into the Trace Pod Data Latch on the Data Acquisition Boards.
PBOVRST	Positive Bus Overview Reset -- developed from HOVS. PBOVRST is used only on the 20 Channel Data Acquisition Board. When PBOVRST goes from a low state to a high state, the 20 Bit Overview Counter is reset.
PBPLS	Positive Bus Pipeline Strobe -- same as HPLS except buffered. Used in the 20 and 40 Channel Data Acquisition Boards for latching information into Pipeline Registers at the correct time in the Analyzer's timing cycle.
PBRSTB	Positive Bus Read Strobe -- a CPU generated signal. When PBRSTB goes from a low state to a high state, P(N)DSTB, P(N)MACRS and P(N)SQRGS are enabled in the Strobe Generator. These strobes are used to latch internal information into various data registers/memories as it moves from the input of the State Analyzer to the its outputs and then to the CPU.
PBSRS	Positive Bus State Recognition Strobe -- a differential strobe (NBSRS) developed in the Strobe Generator, and sent to the Data Acquisition Boards. At the beginning of a data acquisition cycle, PBSRS goes from a low state to a high state. PBSRS is used to latch user information into the State Recognition Latches/Counters.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
PBSTBRQ	Positive Bus Strobe Request -- a signal coming from the Data Acquisition Boards during Performance Verification only. PBSTBRQ when going from a low to a high state, begins a strobe generator cycle. PBSTBRQ is wire ORed with PPVSTB and HMCLK.
PDC	Positive Delayed Clock -- an IMB signal driven by the State Analyzer. PDC is a delayed version of HMCLK. When enabled, PDC may be used by other Modules using the IMB.
PDSTB	Positive Data Strobe -- a differential signal (NDSTB) developed in the Strobe Generator. PDSTB and NDSTB are used to develop HDVLD (see HDVLD).
PHALT	Positive Halt -- PHALT goes from a low to a high state when Trace Point or Measurement Complete occurs, if enabled by the user. PHALT is used in the Preprocessor (if enabled) and becomes PORT2.
PIHALT	Positive Interface Halt -- a differential signal (NIHALT) sent to the Preprocessor that can be used to halt the user's system. PIHALT is derived from PHALT when enabled by HENHLT.
PISTIM	Positive Interface Stimulus -- a differential signal (NISTIM) sent to the Preprocessor. PISTIM is developed from PSTIM when enabled by HENSTIM. PISTIM goes from a low to a high state when a Trigger Event or Sequence Event occurs if enabled by the user.
PMACRS	Positive Memory Address Counter Register Strobe -- a differential signal (NMACRS) developed in the Strobe Generator. PMACRS is used to latch information from the Trace Count/Status Memory Address Counter into the Trace Memory Address Counter Read Register. The information in the Register is transferred to the CPU Data Bus when LRMACR goes low.
PORT1	Port 1 -- a signal from the Card Cage to the Rear Panel Connector PORT 1. In the case of the State Analyzer Control Board, PORT1 is used for Positive Stimulus (see PSTIM).
PORT2	Port 2 -- a signal from the Card Cage to the Rear Panel Connector PORT 2. In the case of the State Analyzer Control Board, PORT2 is used for Positive Halt (see PHALT).
PPLS	Positive Pipeline Strobe -- same as NINCSS but inverted. When PPLS goes from a low to a high state, the Sequence Pipeline Latch/Counter is incremented one state when in the count mode.
PPVSTB	Positive Performance Verification Strobe -- PPVSTB is developed in the Write Decoders from the CPU. PPVSTB when going from a low state to a high state begins a strobe generator cycle. PPVSTB is used only during Performance Verification. PPVSTB is wire ORed with HMCLK and PBSTBRQ.
PSOCINC	Positive Sequence Occurrence Counter Increment -- developed from NOCSTB. When PSCINC goes from a low to a high, the Sequence Occurrence Counters

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
	will be incremented one state when in the count mode. PSOCINC may also be driven by HBOWRT, they are wire ORed. PSOCINC never drives HBOWRT.
PSQRGS	Positive Sequence Register Strobe -- a differential signal (NSQRGS) developed in the Strobe Generator. PSQRGS is used to latch information from the Sequence Pipeline Latch/Counters into the Sequence Read Register. The information in the Register is placed on the CPU Data Bus when LRSQRG goes low.
PSTIM	Positive Stimulus -- PSTIM goes from a low to a high state when a Trigger Event or a Sequence Event occurs if enabled by the user. PSTIM is used in the Preprocessor (if enabled), and also becomes PORT1.
PWAC	Positive Write Analysis Controller -- a CPU controlled signal developed in the Write Decoders. When the Analysis Controller is in the load mode (LLD low), PWAC writes LDB0 into the Controller.
PWCLK	Positive Write Clock -- a CPU controlled signal developed in the Write Decoders. PWCLK writes LDB0 and LDB1 into the Clock Term Generator.
PWLOAD	Positive Write Load -- a CPU controlled signal developed in the Write Decoders. When going from a low state to a high state, PWLOAD latches LAB0 into the Load Latch asserting or negating HLD and LLD.
PWRUN	Positive Write Run -- a CPU controlled signal developed in the Write Decoders. When going from a low state to a high state PWRUN latches LAB0 into the Run Latch producing LRUN and latches LAB1 into the Port Latches negating LTP and LMC.
TSS0-7	Trace Sequence State 0-7 -- outputs of the Sequence State Latch/Counters used in either the load mode or the run mode. TSS0-7 represent the present sequence state.
VTHSH1-2	Voltage, Threshold 1-2 -- a voltage that is programmable by the user and sent to the Clock Probe as a reference voltage for the Comparators.

Table 8-2. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

µP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS

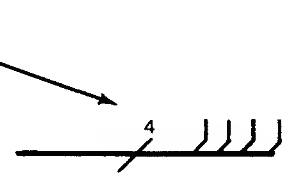


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Table 8-3. Logic Symbology

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

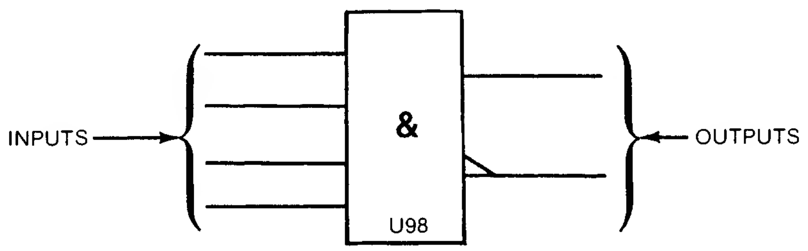
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

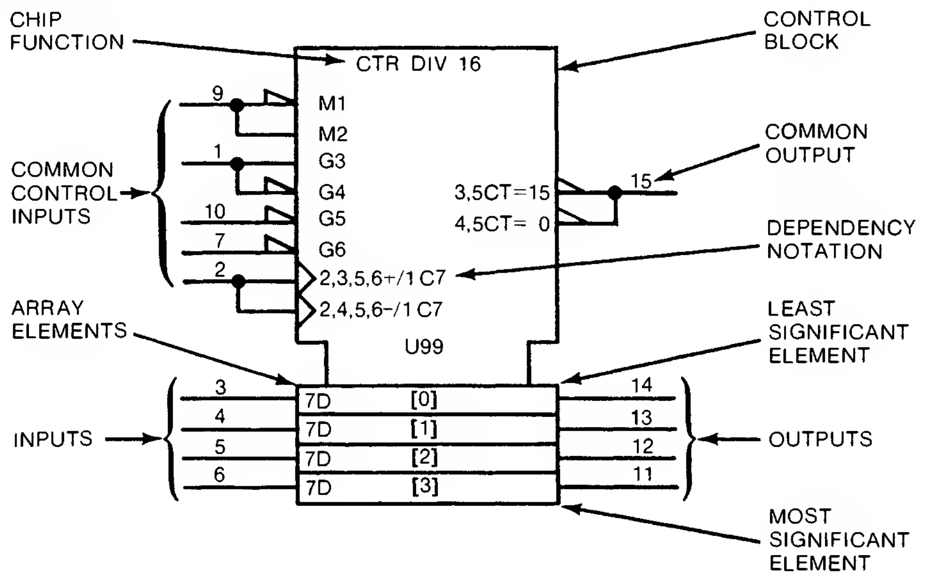
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in [ ]).

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Table 8-3. Logic Symbology (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-3. Logic Symbology (Cont'd)

OTHER SYMBOLS

⌒	Analog Signal	⊵ ⊴	Inversion	→	Shift Right (or down)
&	AND	○	Negation	/	Solidus (allows an input or output to have more than one function)
} {	Bit Grouping	—✕—	Nonlogic Input/Output	▽	Three State
▷	Buffer	◇	Open Circuit (external resistor)	,	Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
!	Compare	◇	Open Circuit (external resistor)	( )	Used for factoring terms using algebraic techniques.
▷	Dynamic	≥1	OR	[ ]	Information not defined.
=1	Exclusive OR	◇	Passive Pull Down (internal resistor)	Φ	Logic symbol not defined due to complexity.
⊓	Hysteresis	◇	Passive Pull Up (internal resistor)		
?	Interrogation	¬	Postponed		
—	Internal Connection	←	Shift Left (or up)		

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

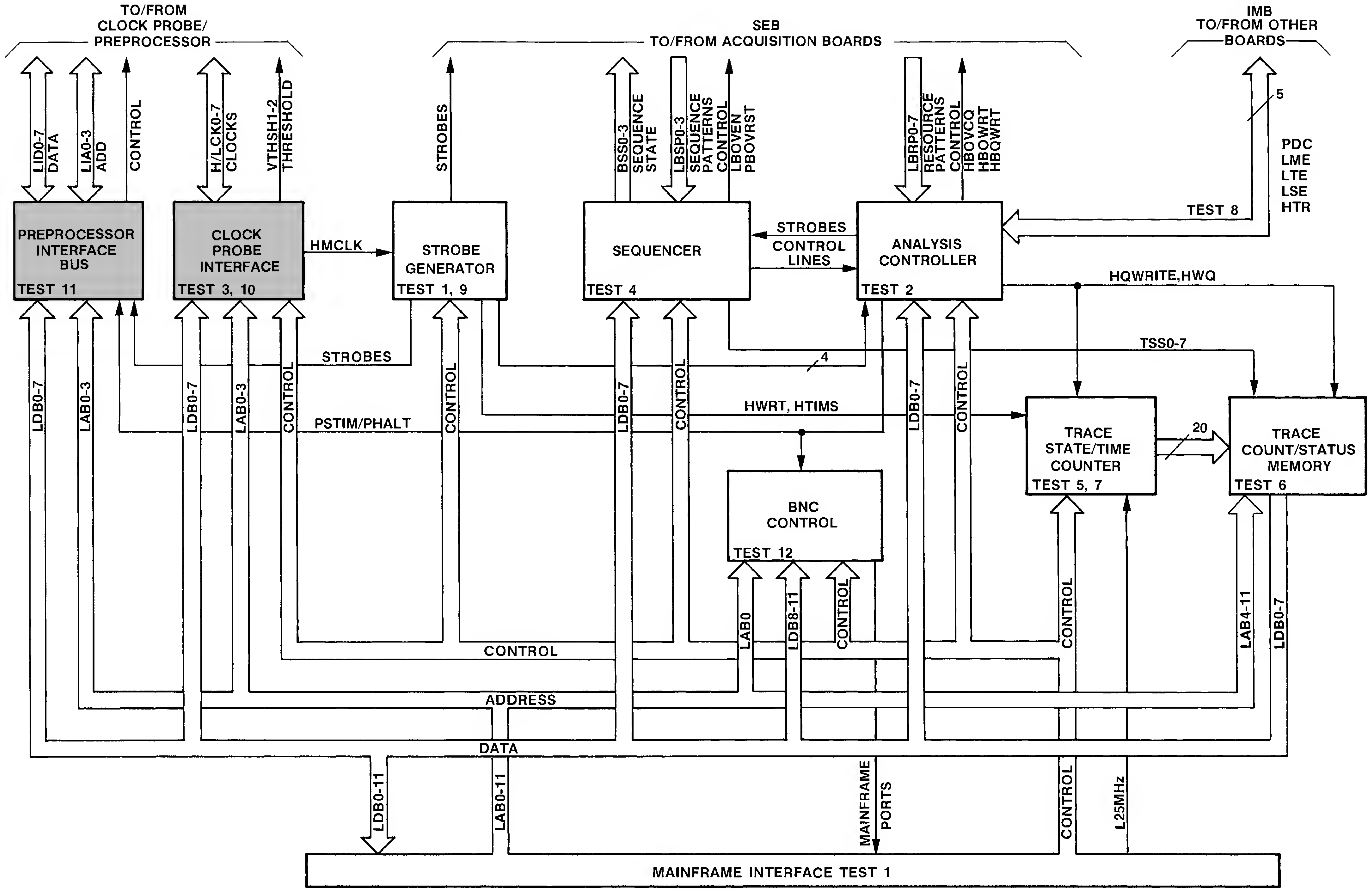
CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

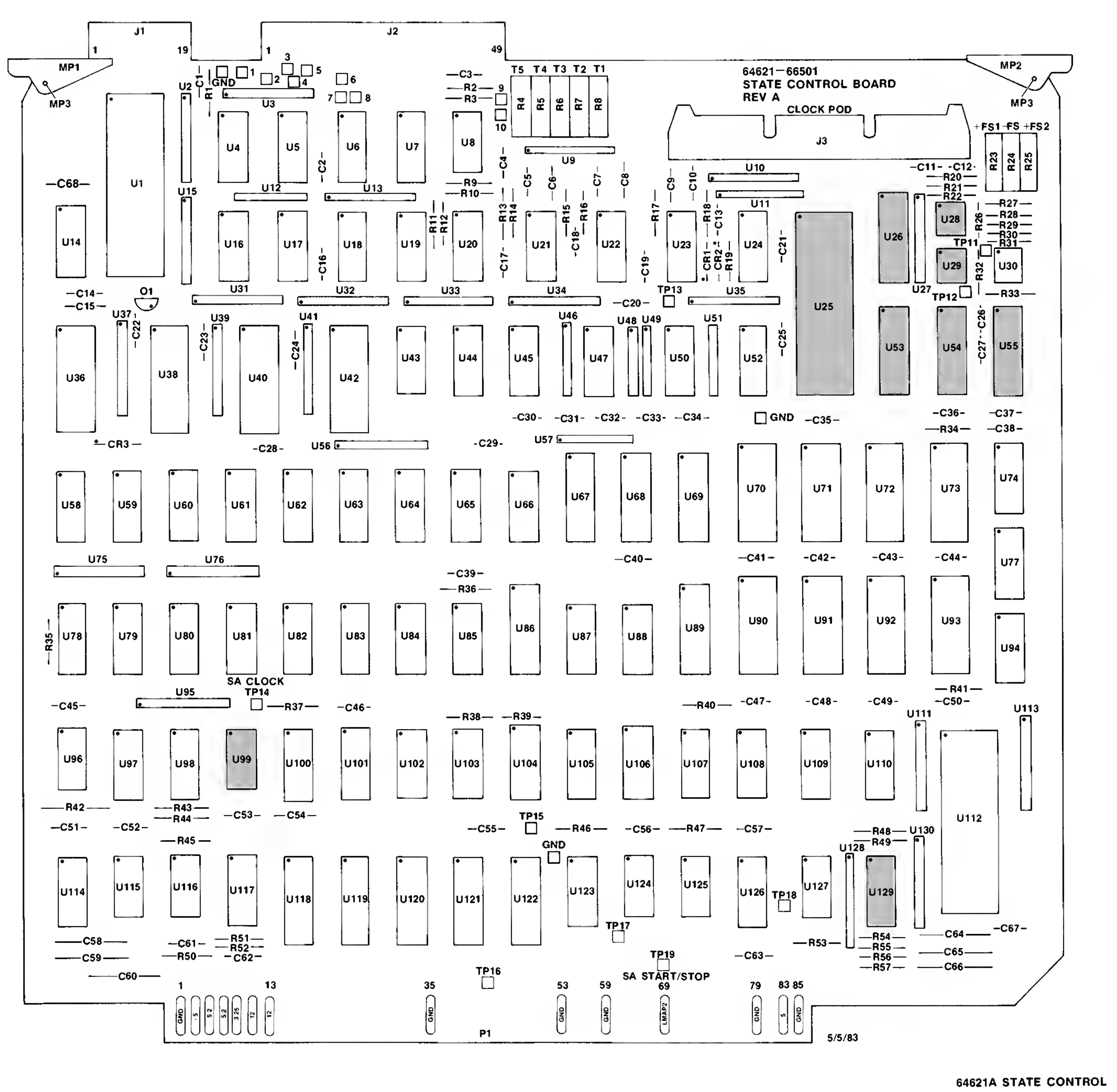
DELAY and MULTIVIBRATORS

⎍⎍	Astable	NV	Nonvolatile
100 ns	Delay	I	State of initial power up
1⎍	Nonretriggerable Monostable	⎍	Retriggerable Monostable

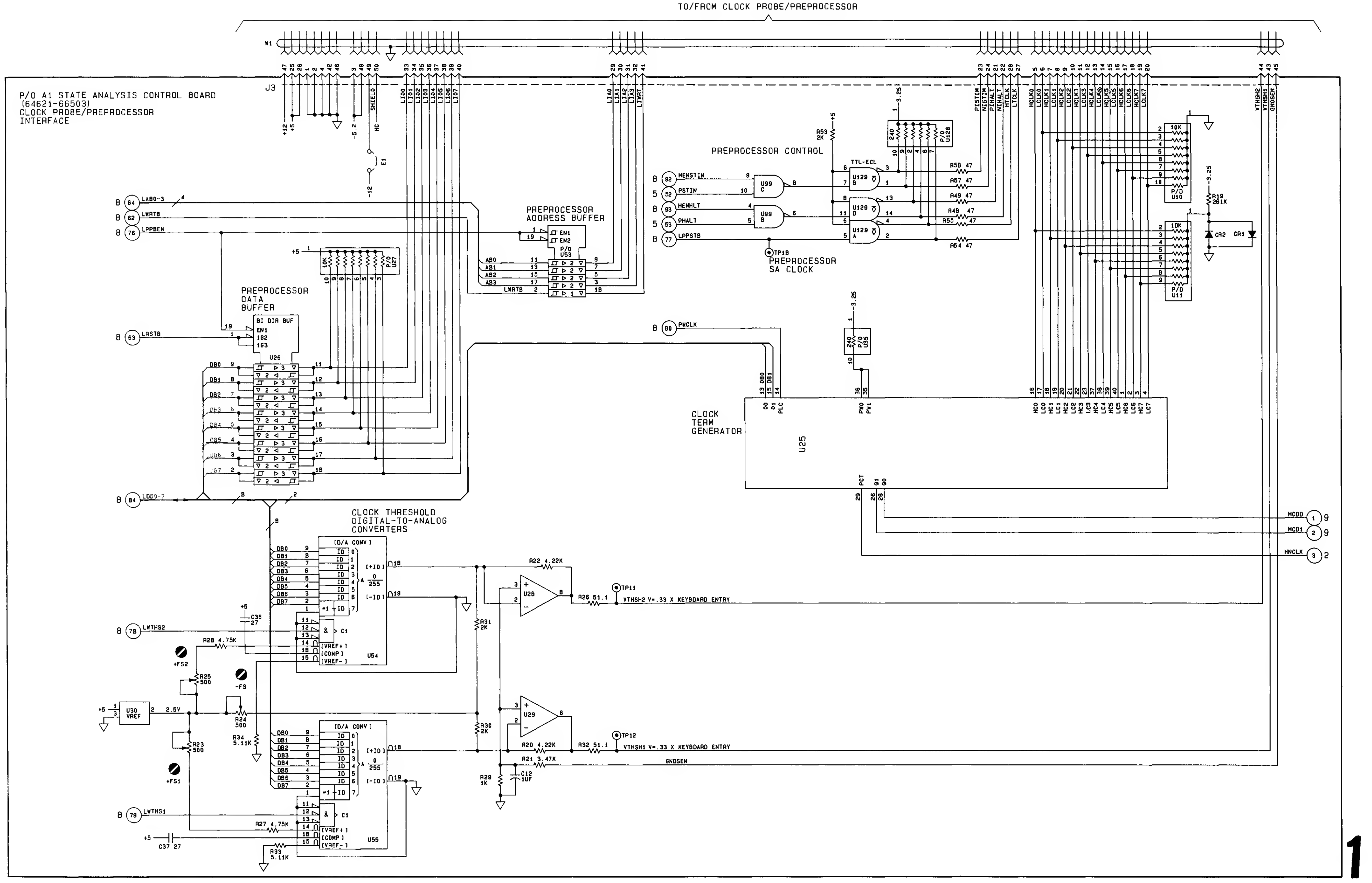
LS-04-08-83 - 3



Block Diagram



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U25	INB4-5011	INB4-5011
U26	1820-2075	74LS245
U28-29	1826-0271	SN72741P
U53	1820-2024	74LS244
U54-55	1826-0856	AM6080APC
U99	1820-1197	74LS00
U129	1820-1173	10124

PARTS ON THIS SCHEMATIC

C12,36,37
CR1,2
J3
R19-34,48,49,54-57
TP11,12
U10,11,25-30,35,53-55,99,128,129
W1

POWER SUPPLY CONFIGURATION

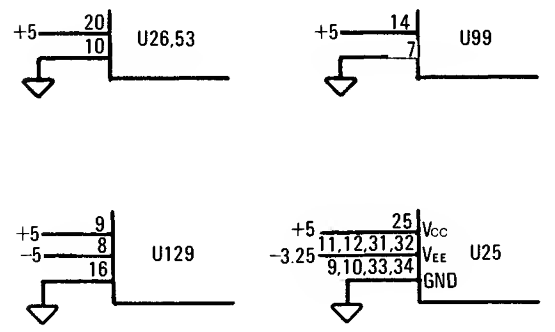
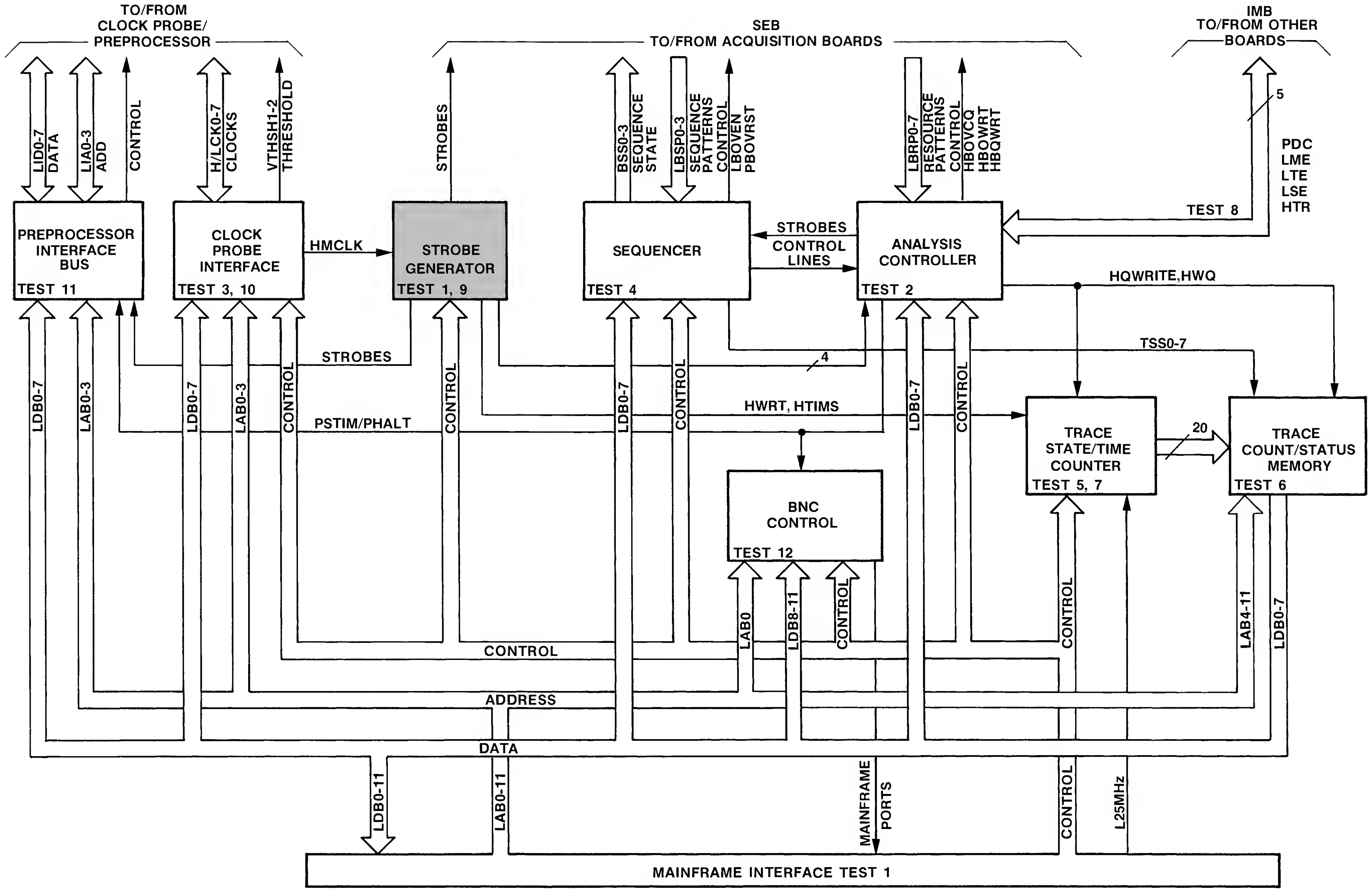
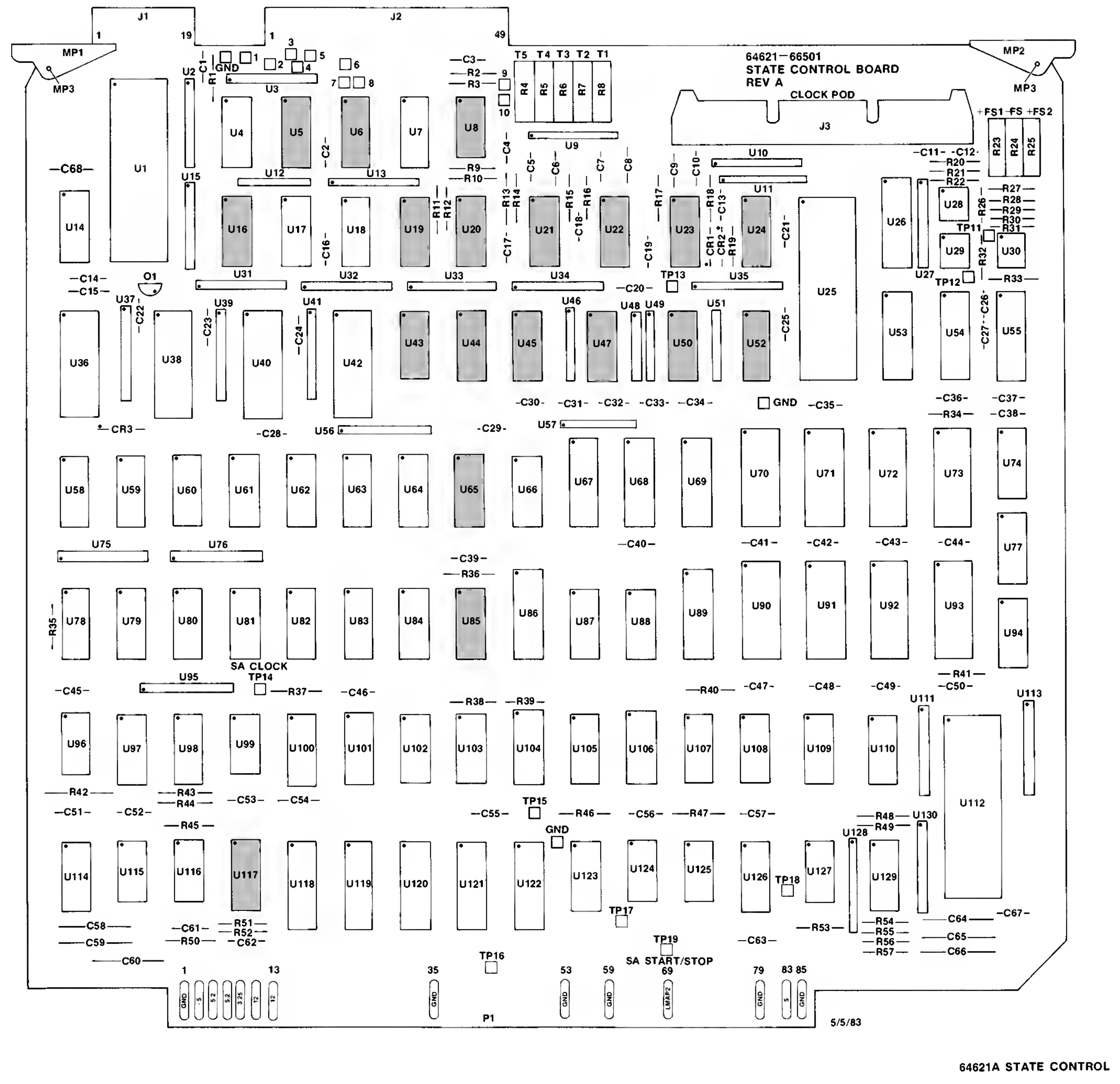


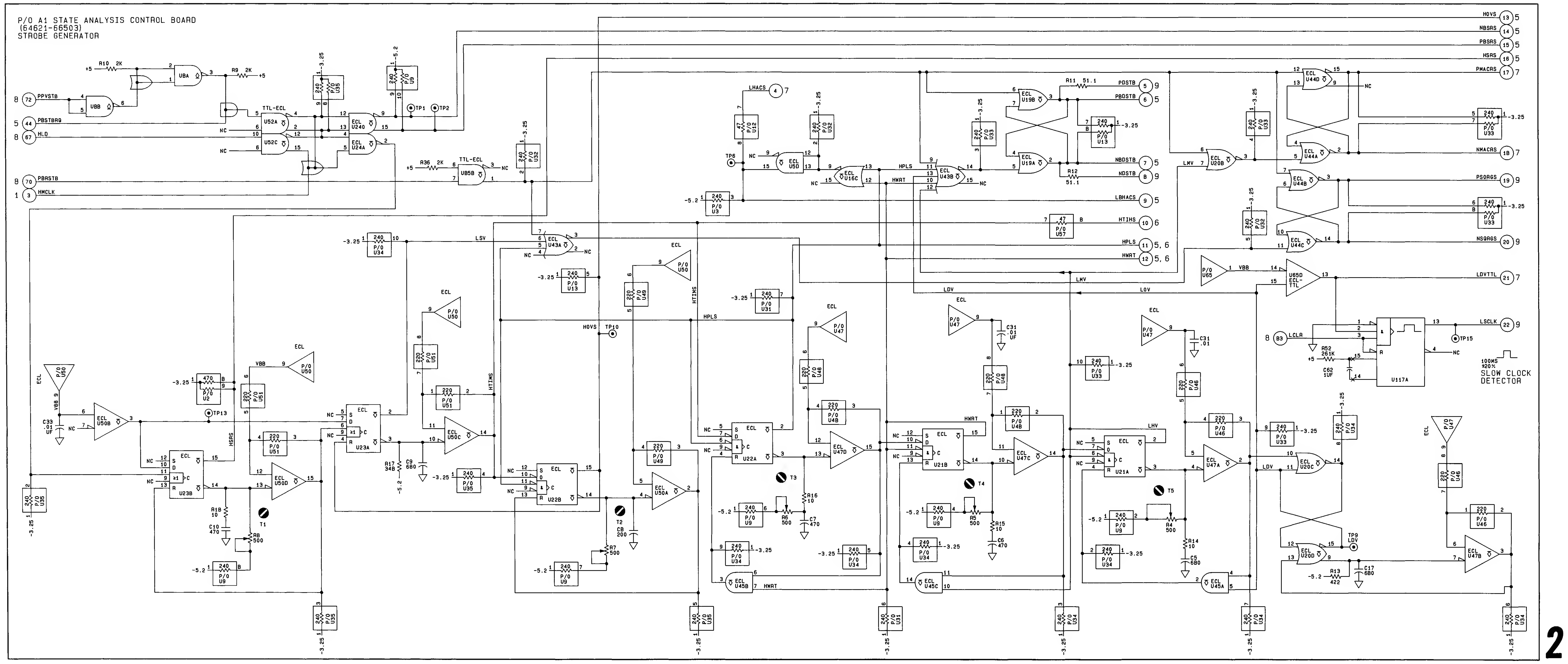
Figure 8-11.
Probe/Preprocessor Interface



Block Diagram



Component Locator



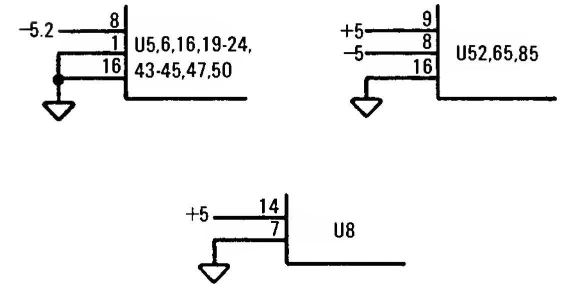
ICs ON THIS SCHEMATIC

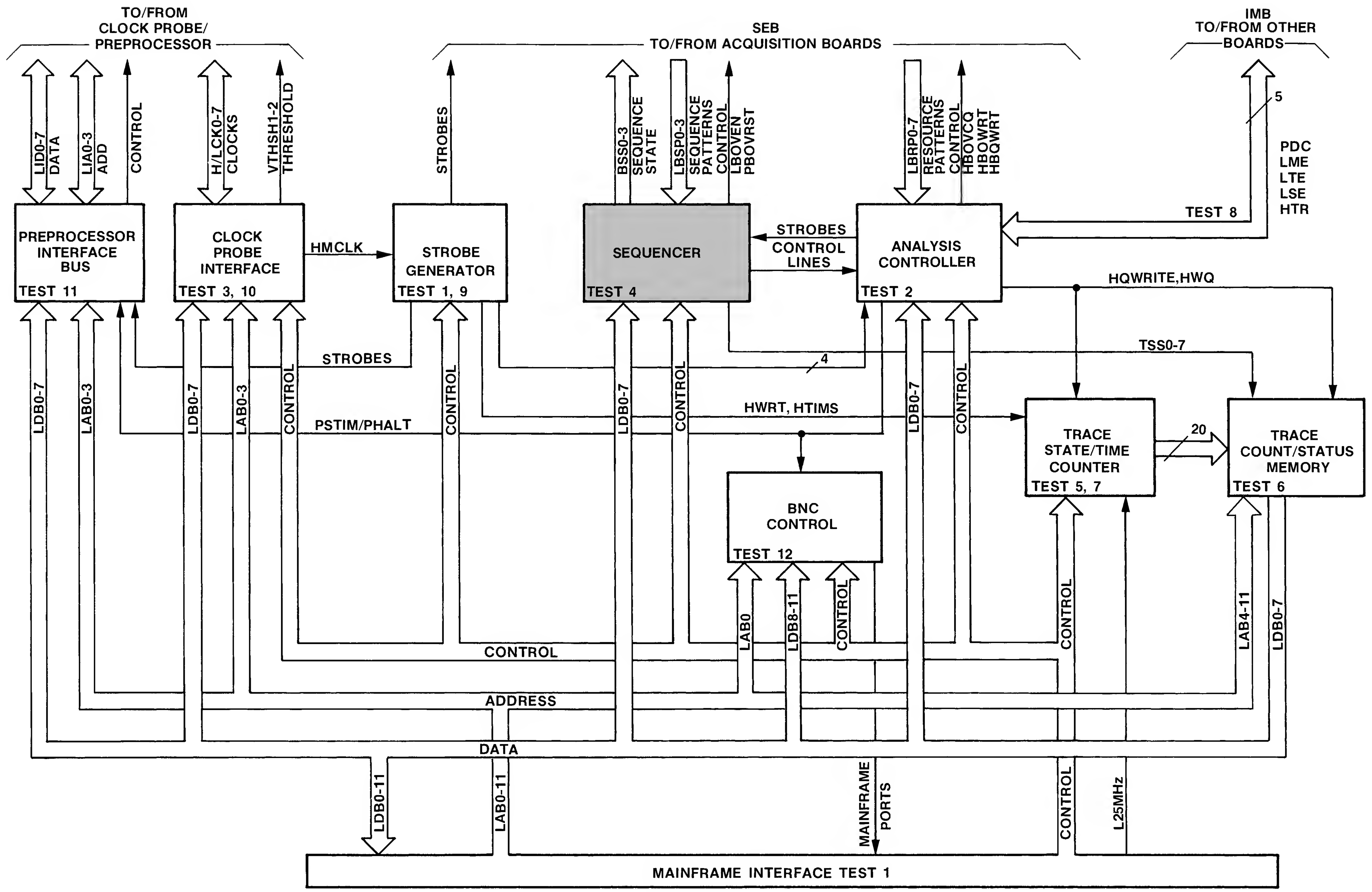
REF. DES.	HP PART NO.	MFG. PART NO.
U5,24,45	1820-1400	10104
U6,19,20,44	1820-0802	10102
U8	1820-0269	7403
U16	1820-1831	10103
U21,22	1820-1944	10130
U23	1820-0817	10131
U43	1820-0806	10109
U47,50	1820-0809	10115
U52,85	1820-1173	10124
U65	1820-1052	10125
U117	1820-1423	74LS123

PARTS ON THIS SCHEMATIC

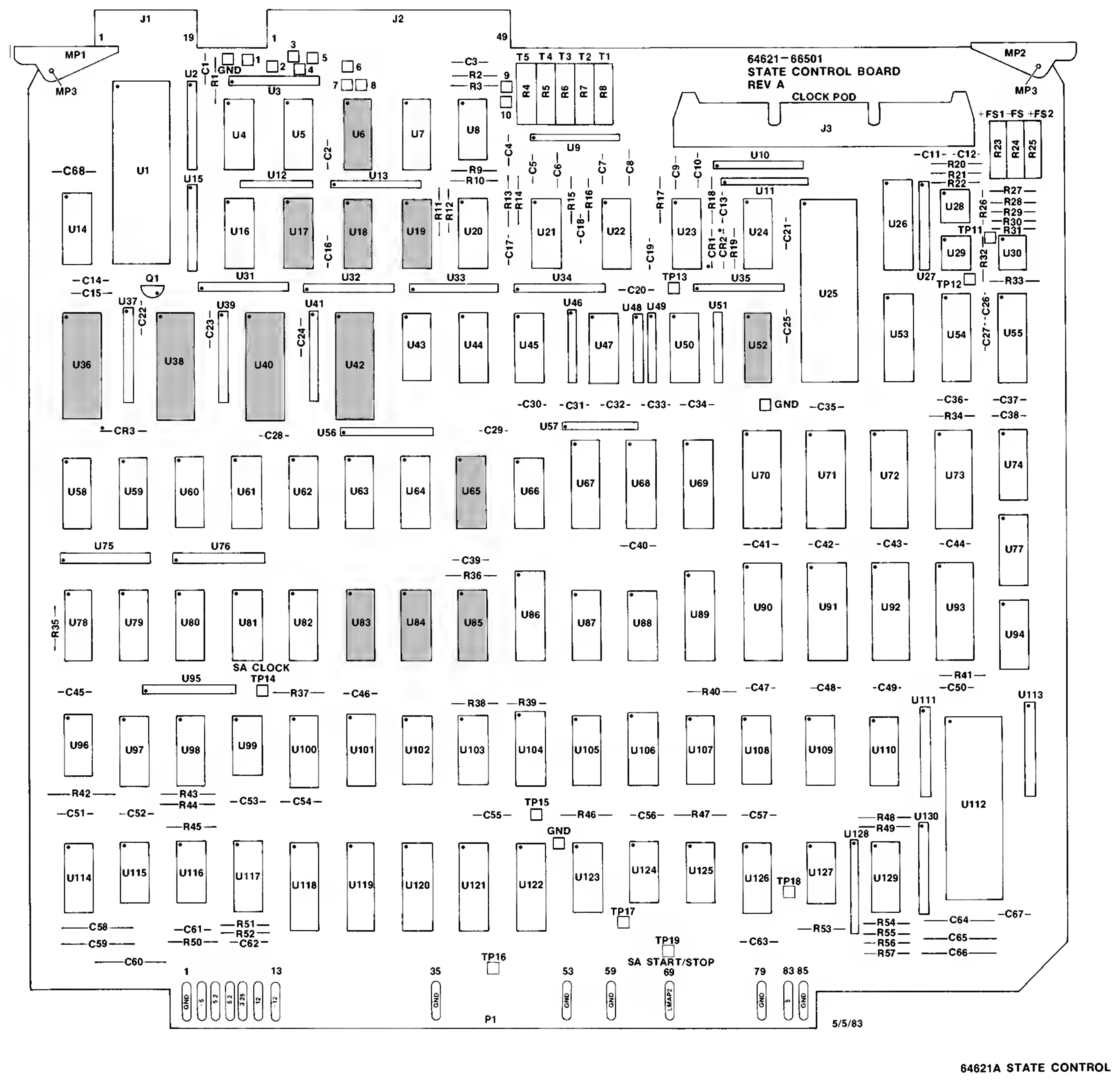
C5-10,17,31,33,62
R4,5,7-18,36,52
TP1,2,6,9,13,15
U2,4-6,8,9,12,13,16,19-24,31-35,43-52,57,65,85,117

POWER SUPPLY CONFIGURATION

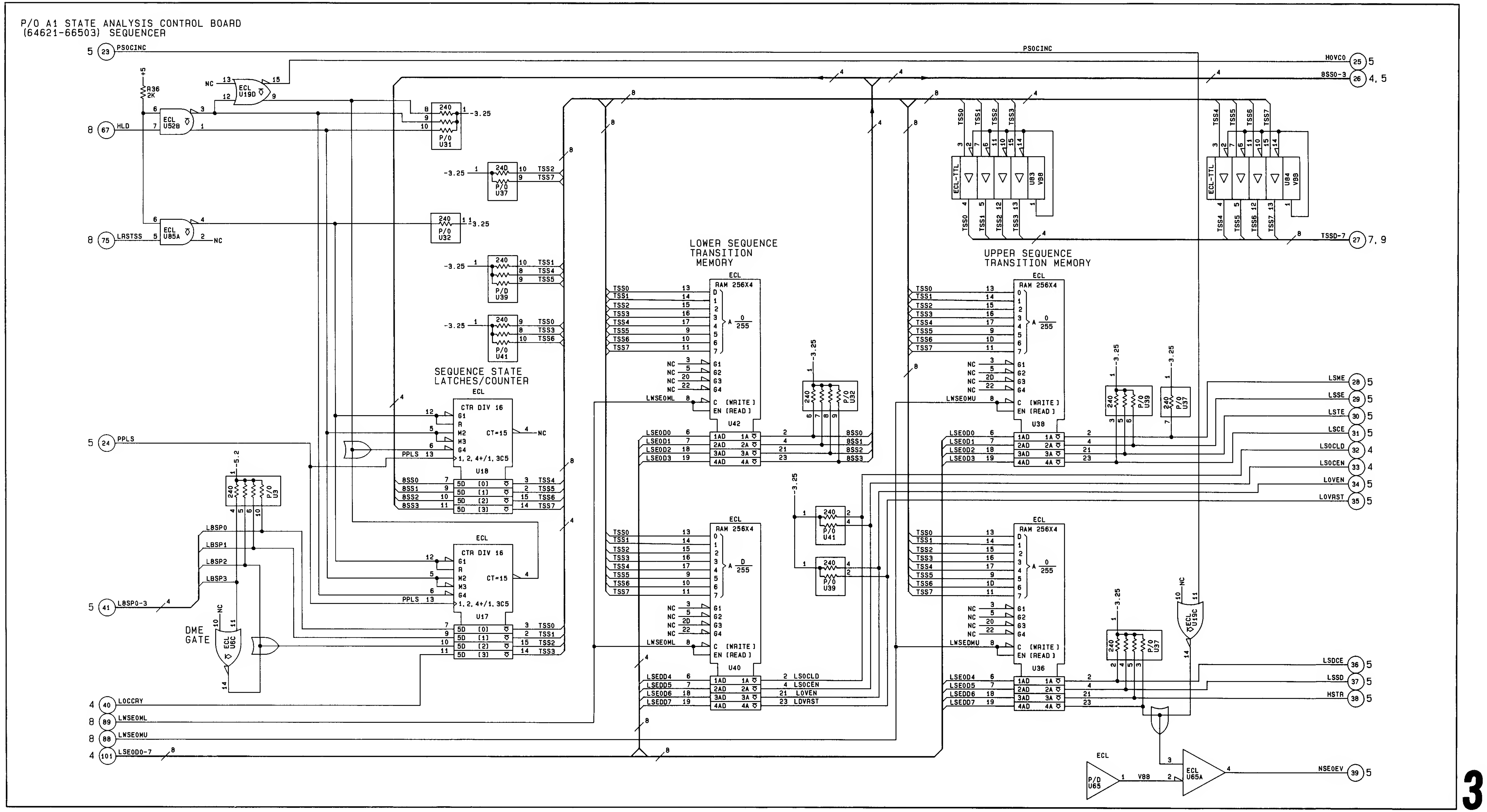




Block Diagram



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U6,19	1820-0802	10102
U17,18	1820-1718	10016
U36,38,40,42	1816-1462	10422
U52,85	1820-1173	10124
U65,83,84	1820-1052	10122

PARTS ON THIS SCHEMATIC

R36
U3,6,17-19,31,32,36-42,52,65,83-85

POWER SUPPLY CONFIGURATION

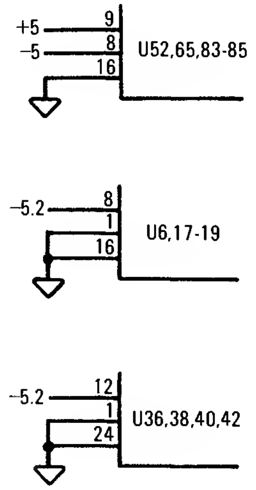
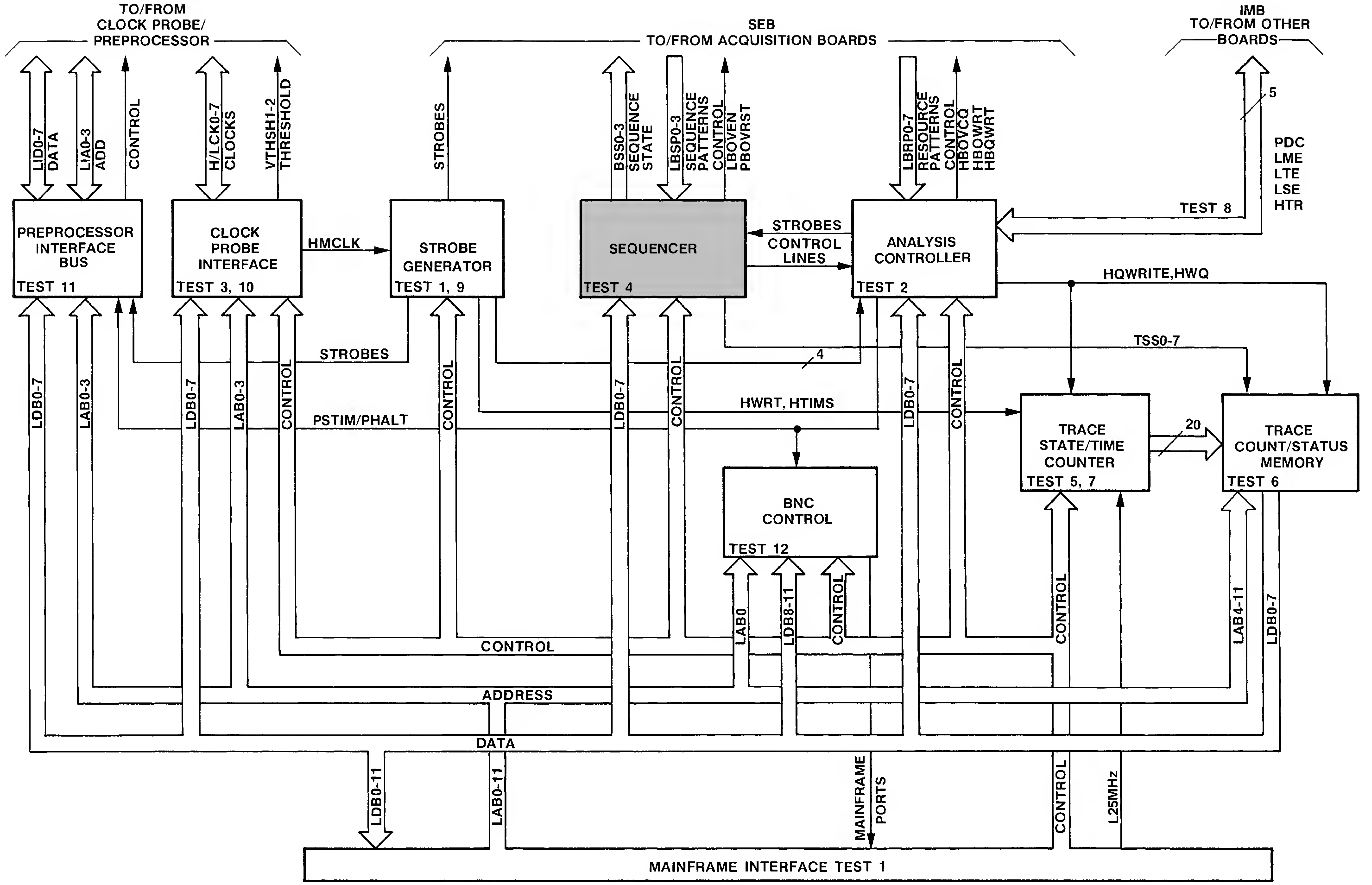
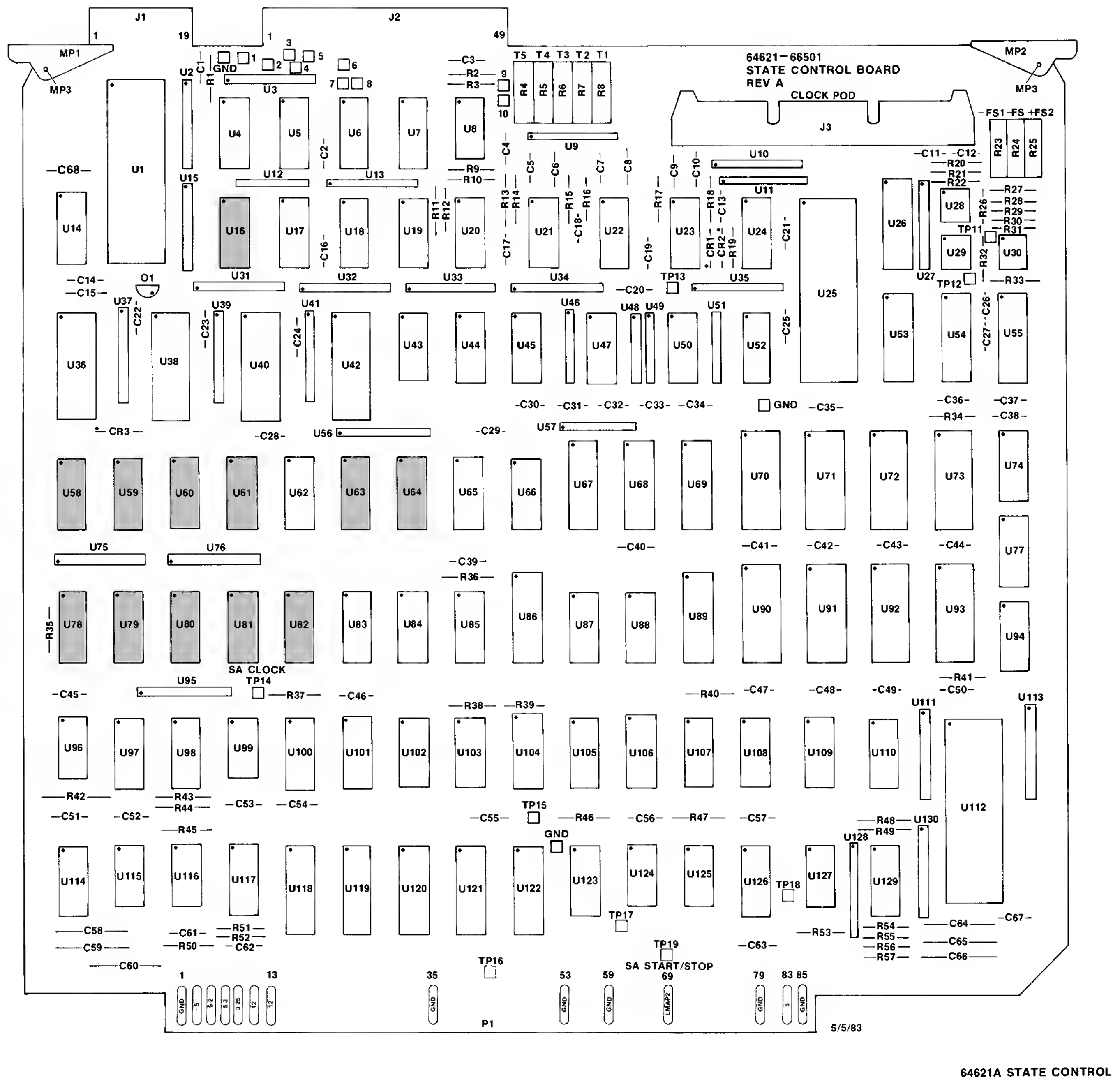


Figure 8-13. Sequencer



Block Diagram



Component Locator

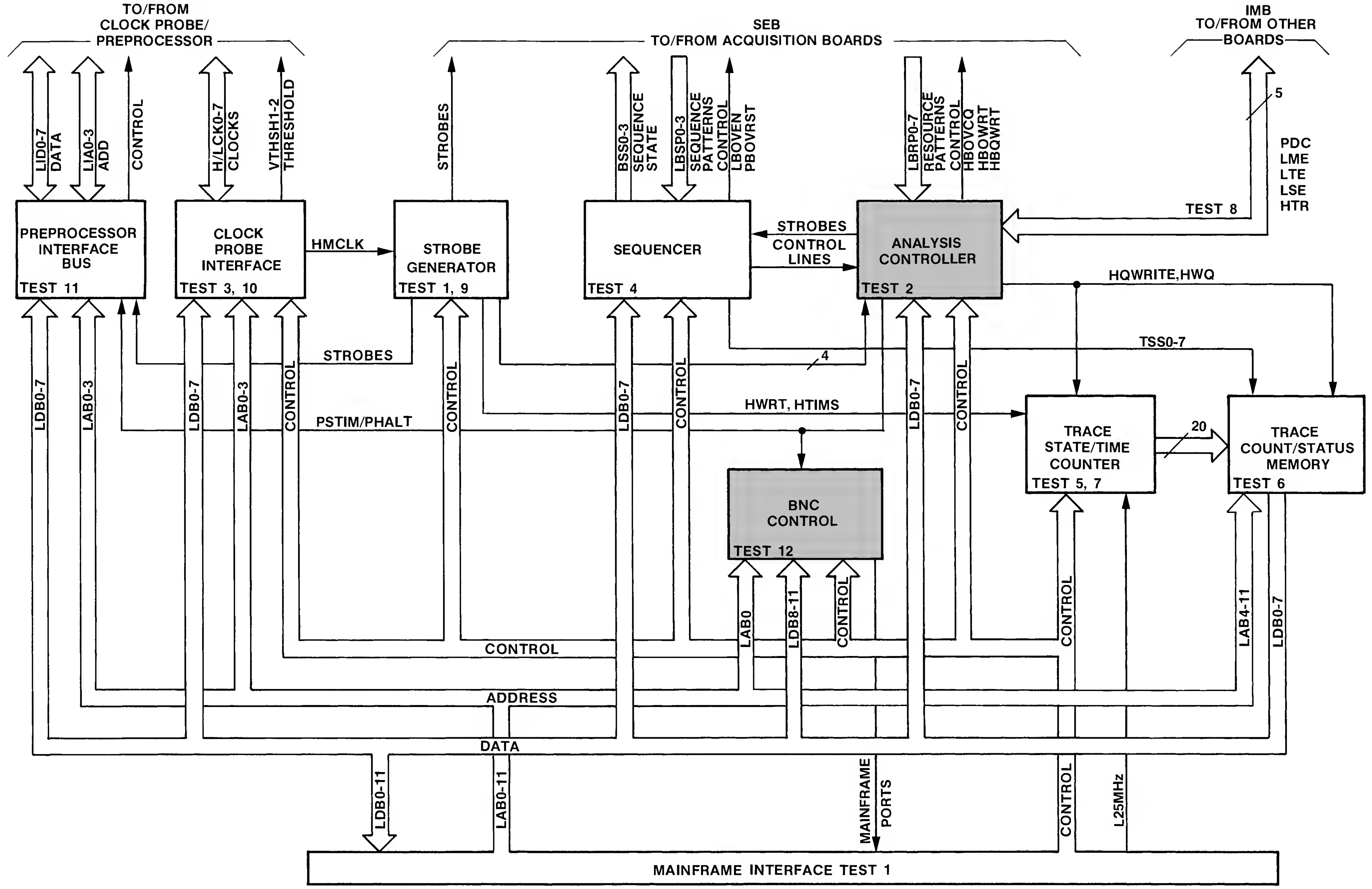
ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U16,80	1820-1831	10103
U58-61	1816-1338	10145
U63-64	1820-1173	10124
U78,79,81,82	1820-1788	10016

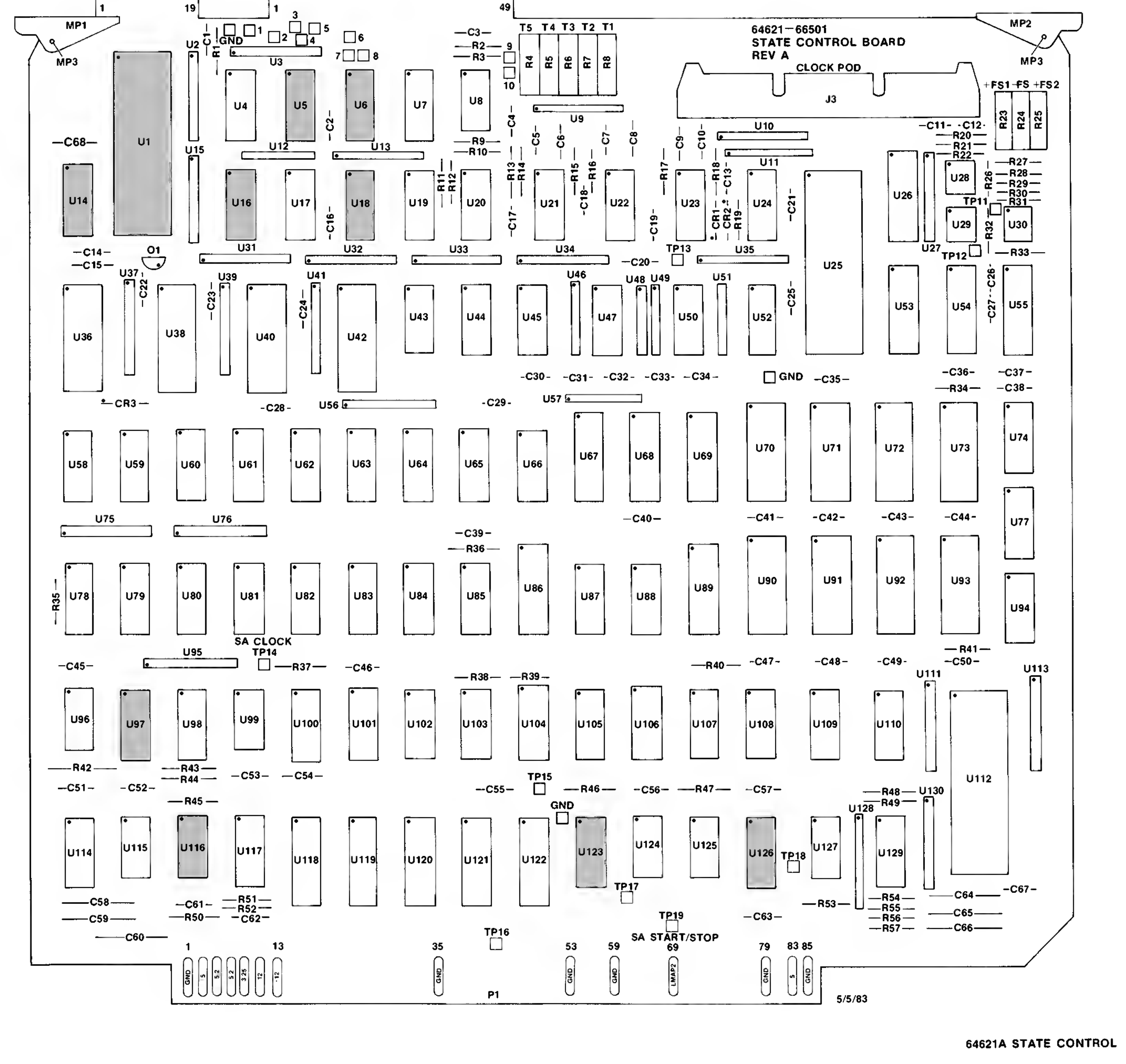
PARTS ON THIS SCHEMATIC

R36
U16,31,41,56,58-61,63,64,75,76,78-82,95

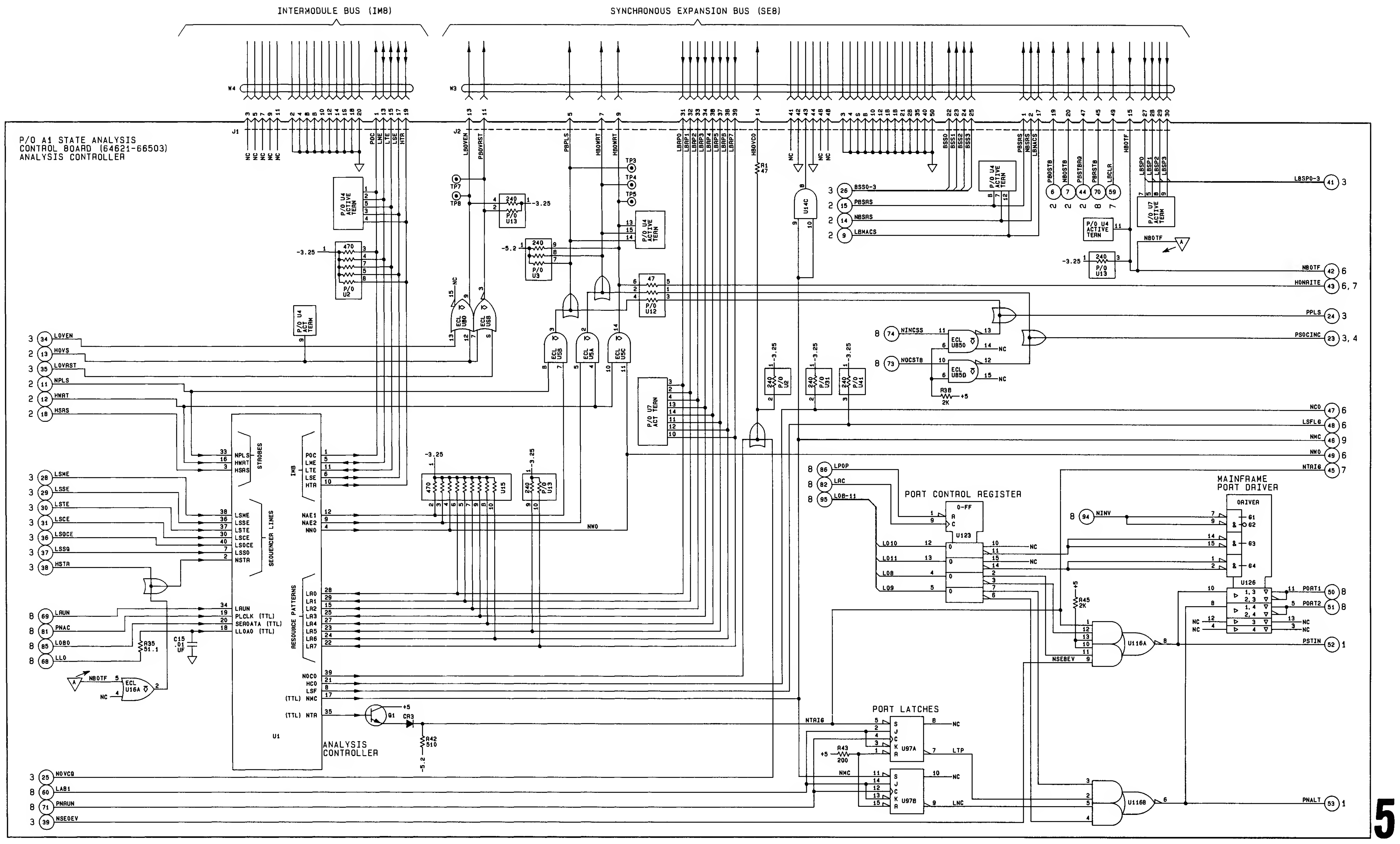
Figure 8-14.
Sequence Occurrence Counter/Memory



Block Diagram



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U1	INB4-5010	INB4-5010
U5	1820-1400	10104
U6	1820-0802	10102
U14	1820-1201	74LS08
U16	1820-1831	10103
U18	1820-1788	10016
U97	1820-1282	74LS109
U116	1820-1210	74LS51
U123	1820-1195	74LS175
U126	1820-0780	AM8831

PARTS ON THIS SCHEMATIC

C15
CR3
J1,2
Q1
R1,35,42,43,45
TP3-5,7,8,10
U1-7,12,13,14,15,16,18,31,41,97,116,123,126

POWER SUPPLY CONFIGURATION

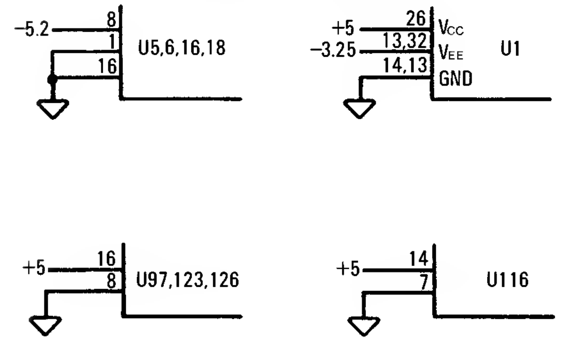
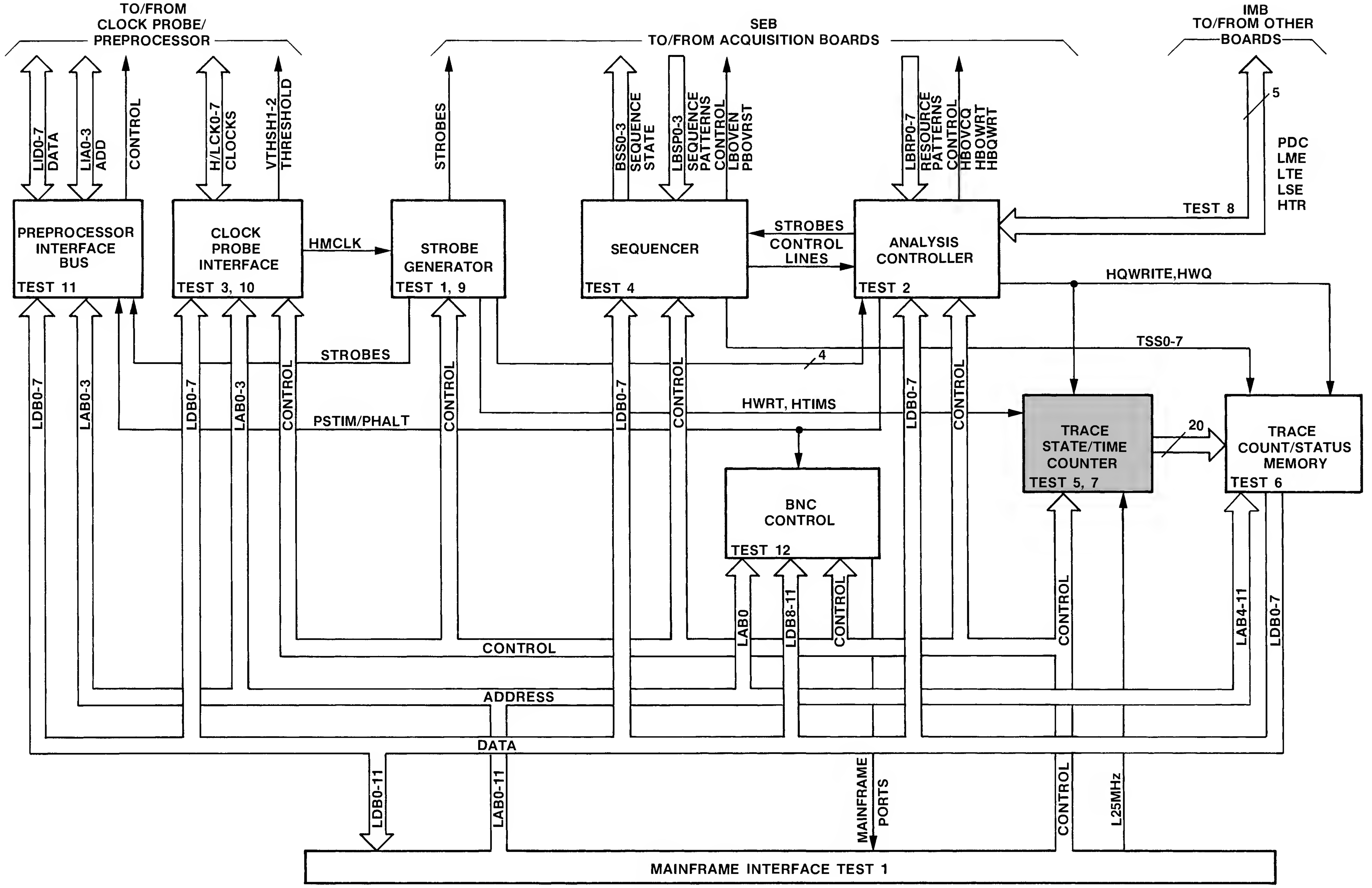
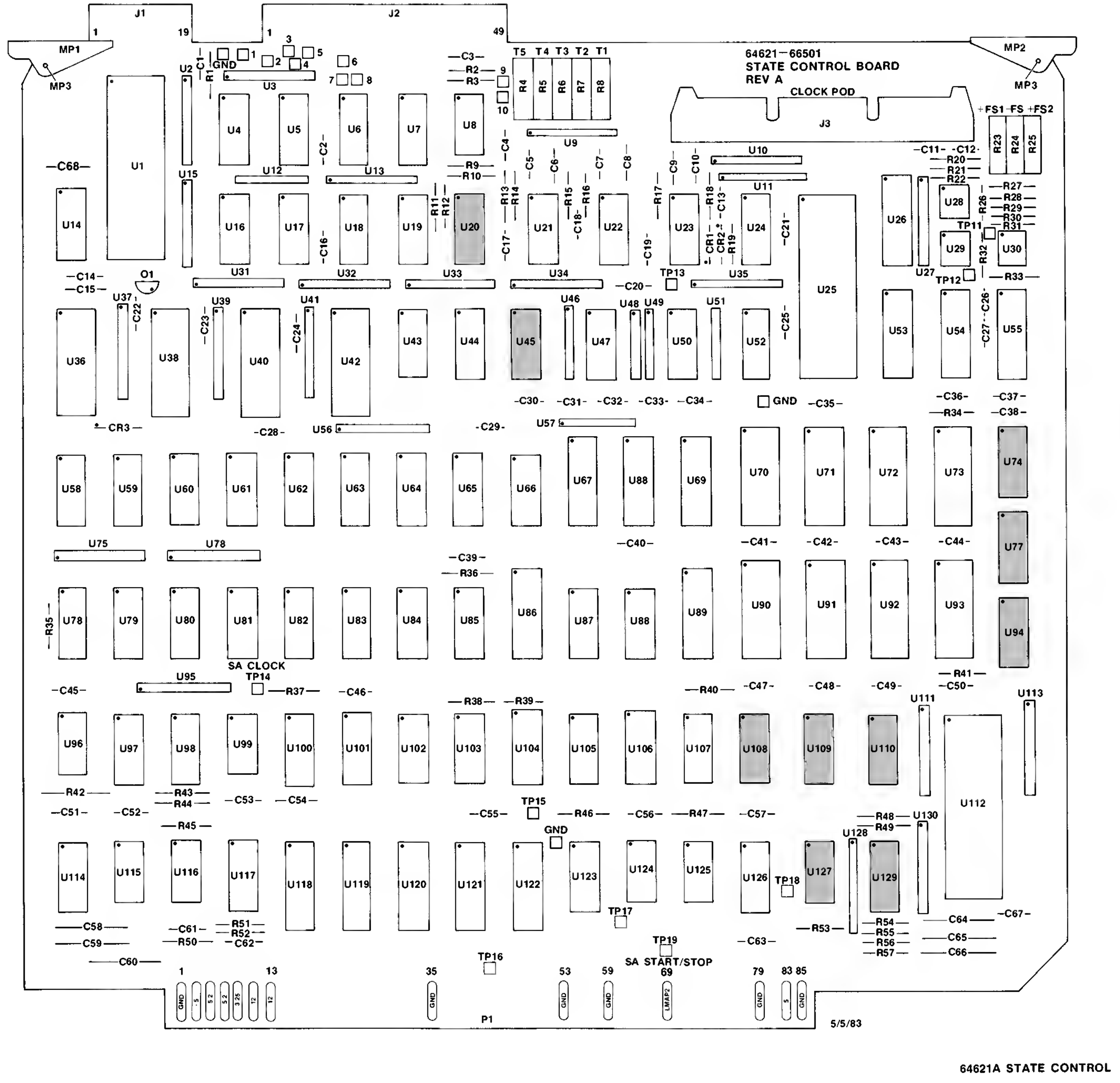


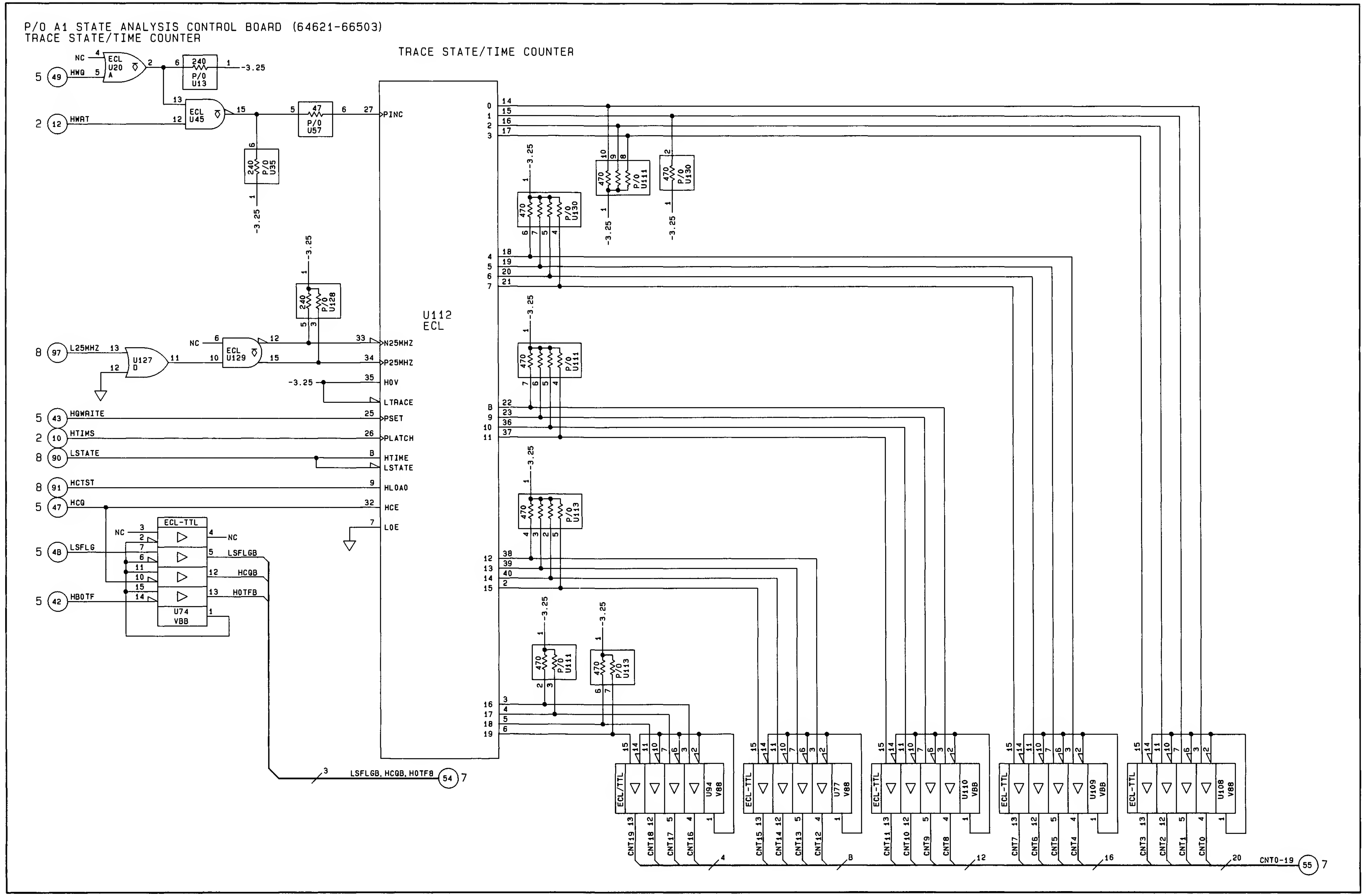
Figure 8-15.
Analysis Controller



Block Diagram



Component Locator



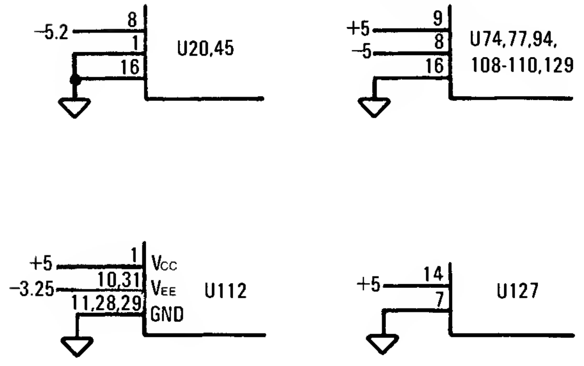
ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U20	1820-0802	10102
U45	1820-1400	10104
U74,77,94, 108,109,110	1820-1052	10125
U127	1920-1208	74LS32
U129	1820-1173	10124

PARTS ON THIS SCHEMATIC

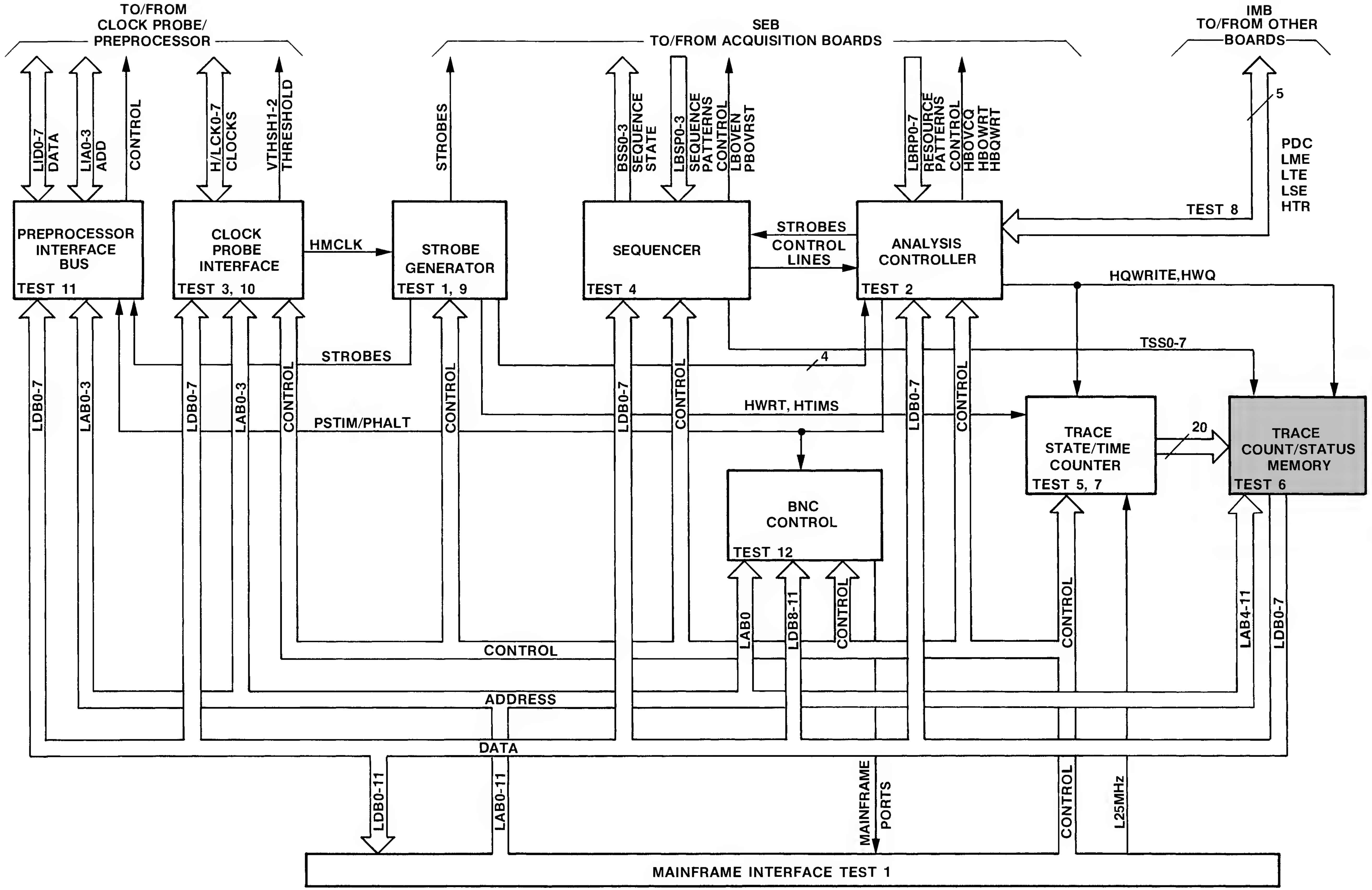
U13,20,35,45,57,74,77,94,108-113,127-130

POWER SUPPLY CONFIGURATION

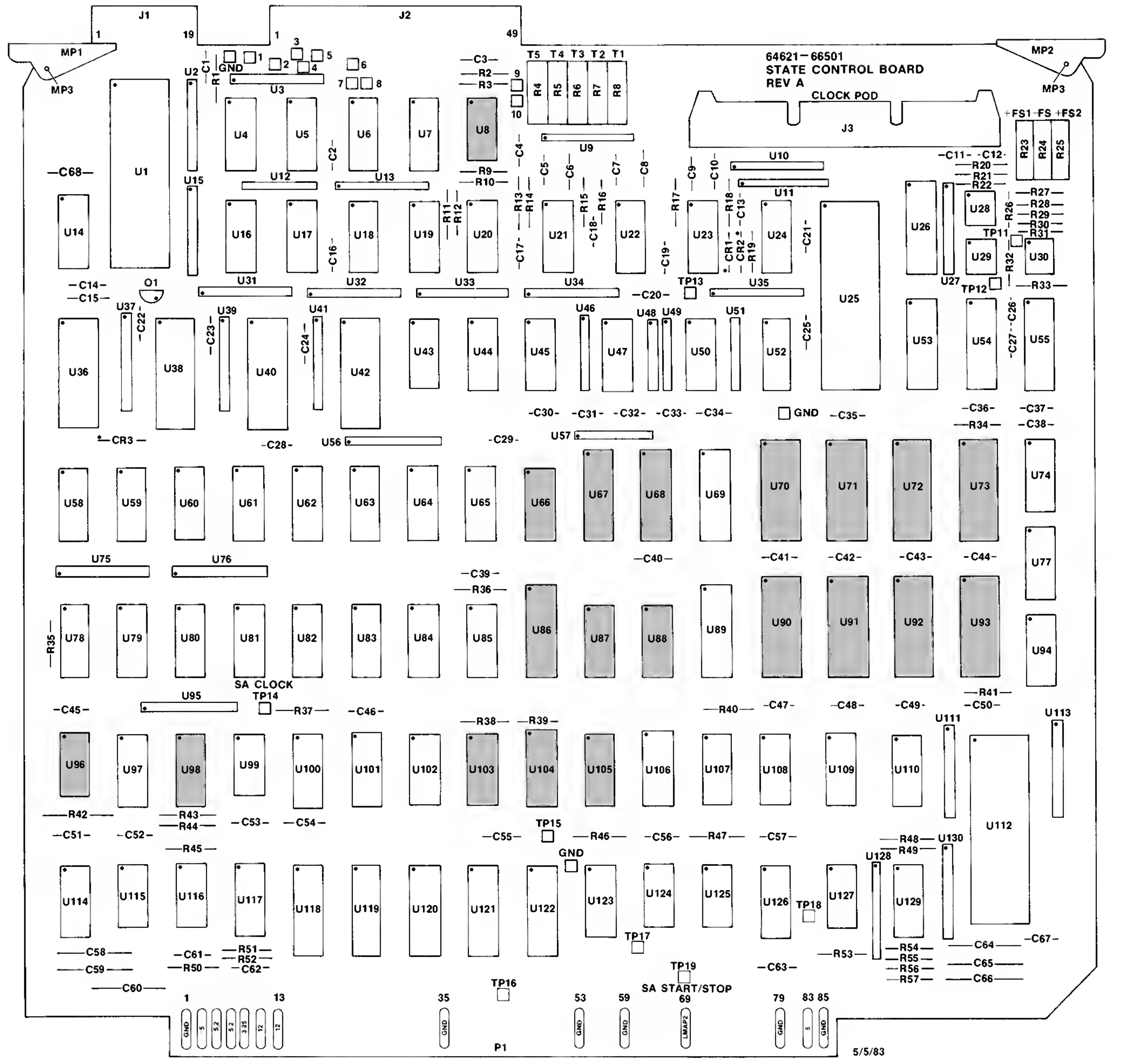


6

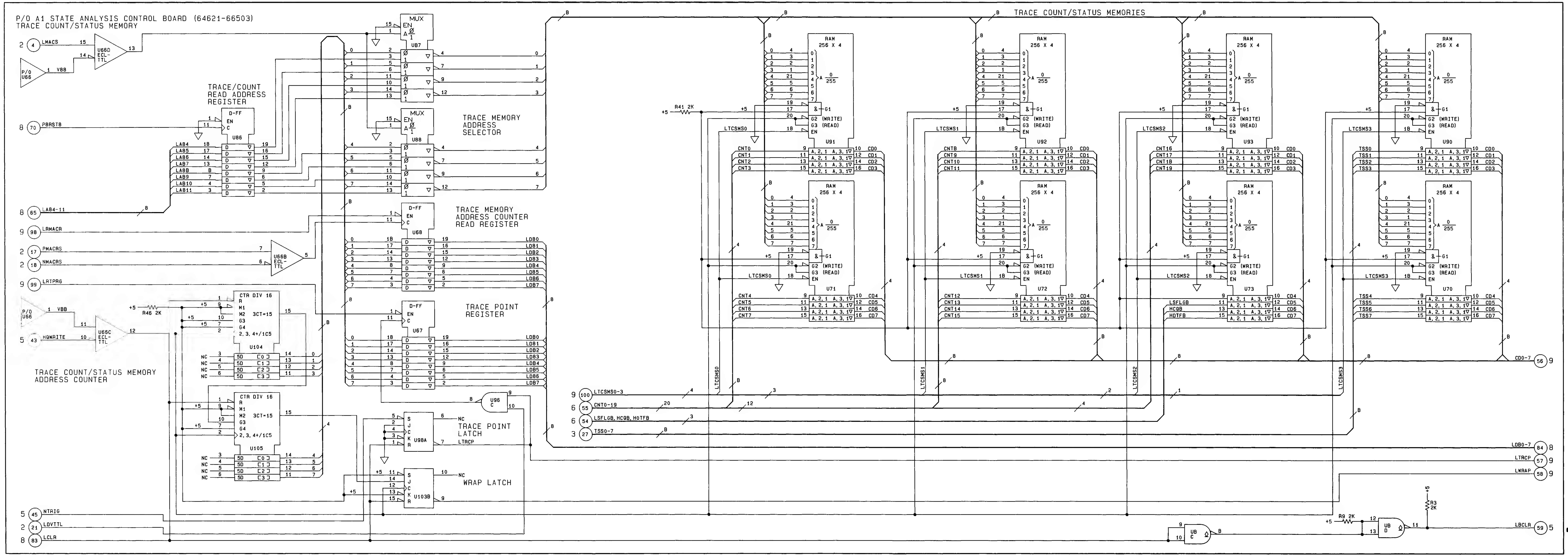
Figure 8-16. Trace State/Time Counter



Block Diagram



Component Locator



7

ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U8	1820-0269	7403
U66	1820-1052	10125
U67,68,86	1820-1997	74LS374
U70-73		
90-93	1816-1308	93LS422
U87,88	1820-1428	74LS158
U96	1820-1197	74LS00
U98,103	1820-1282	74LS109
U104,105	1820-1430	744LS161

PARTS ON THIS SCHEMATIC

R39,41,46
U8,66-68,70-73,86-88,90-93,96,98,103-105

POWER SUPPLY CONFIGURATION

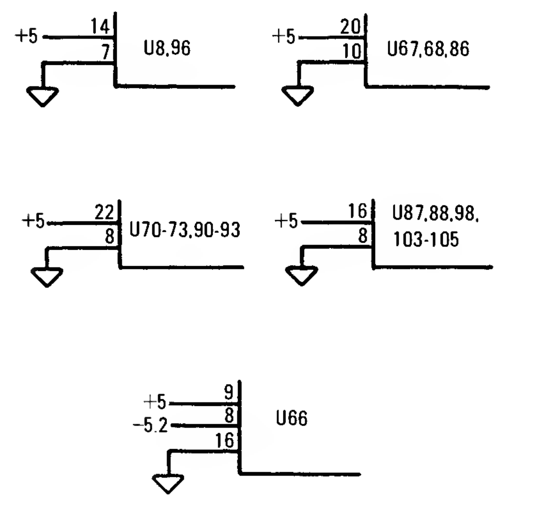
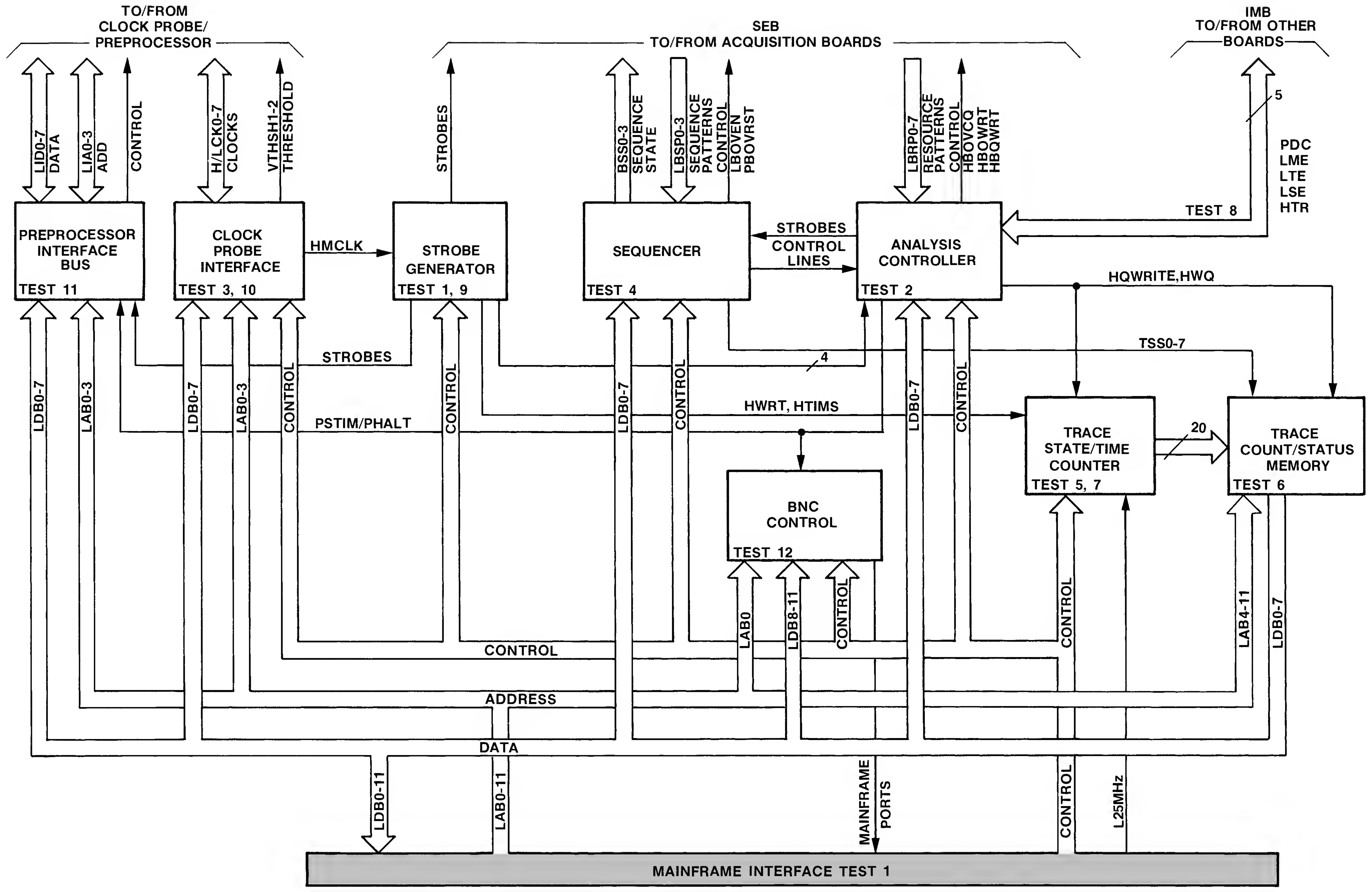
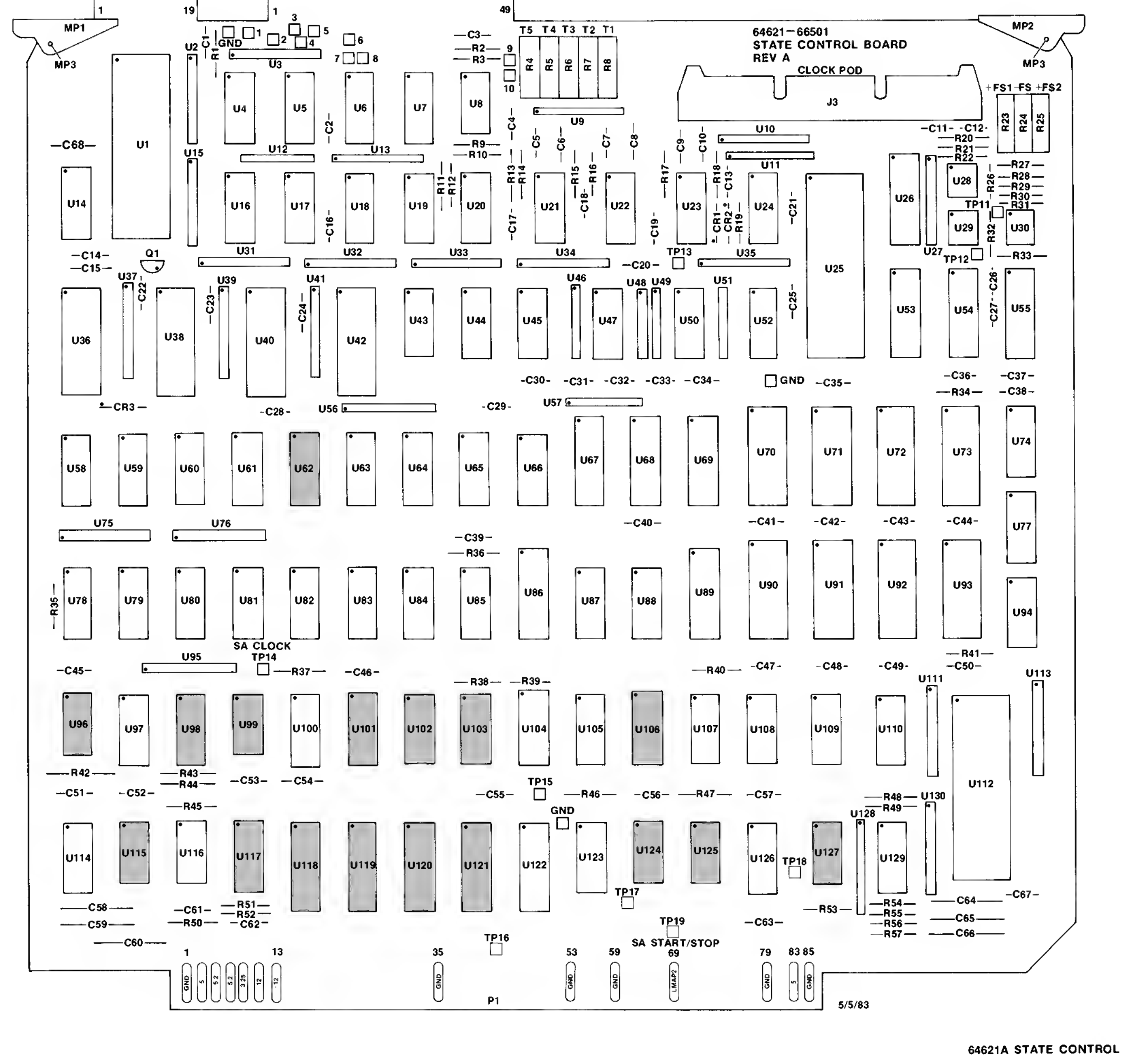


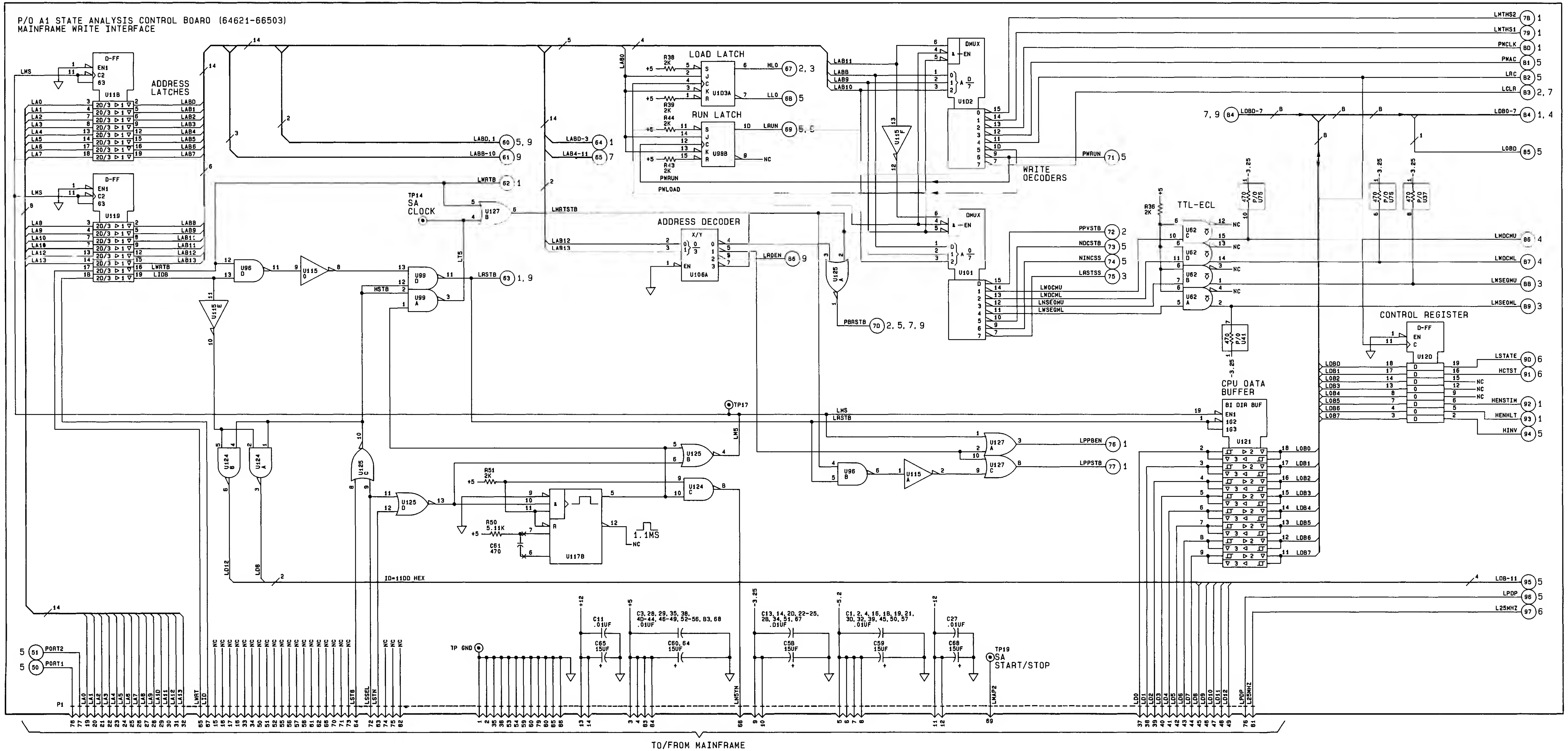
Figure 8-17. Trace Count/Status Memory



Block Diagram



Component Locator



8

ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U62	1820-1173	10124
U96,99	1820-1197	74LS00
U98,103	1820-1282	74LS109
U101,102	1820-1216	74LS138
U106	1820-1281	74LS139
U115	1820-1199	74LS04
U117	1820-1423	74LS123
U118,119	1820-2102	74LS373
U120	1820-1997	74LS374
U121	1820-2075	74LS245
U124	1820-0269	7403
U125	1820-1144	74LS02
U127	1820-1208	74LS32

PARTS ON THIS SCHEMATIC

C1-4,11,13,14,16,18-30,32,34,35,38-59,61,63,65-67
P1
R36,38,39,43,44,50,51
TP17,18
U37,41,62,75,76,96,98,99,101-103,106,
115,117-121,124,125,127

POWER SUPPLY CONFIGURATION

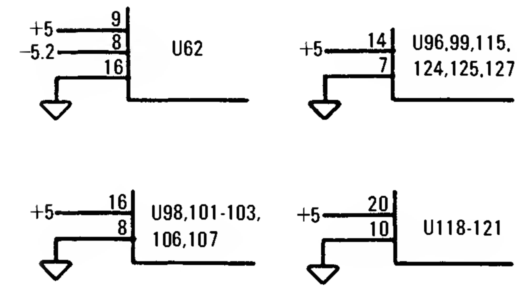
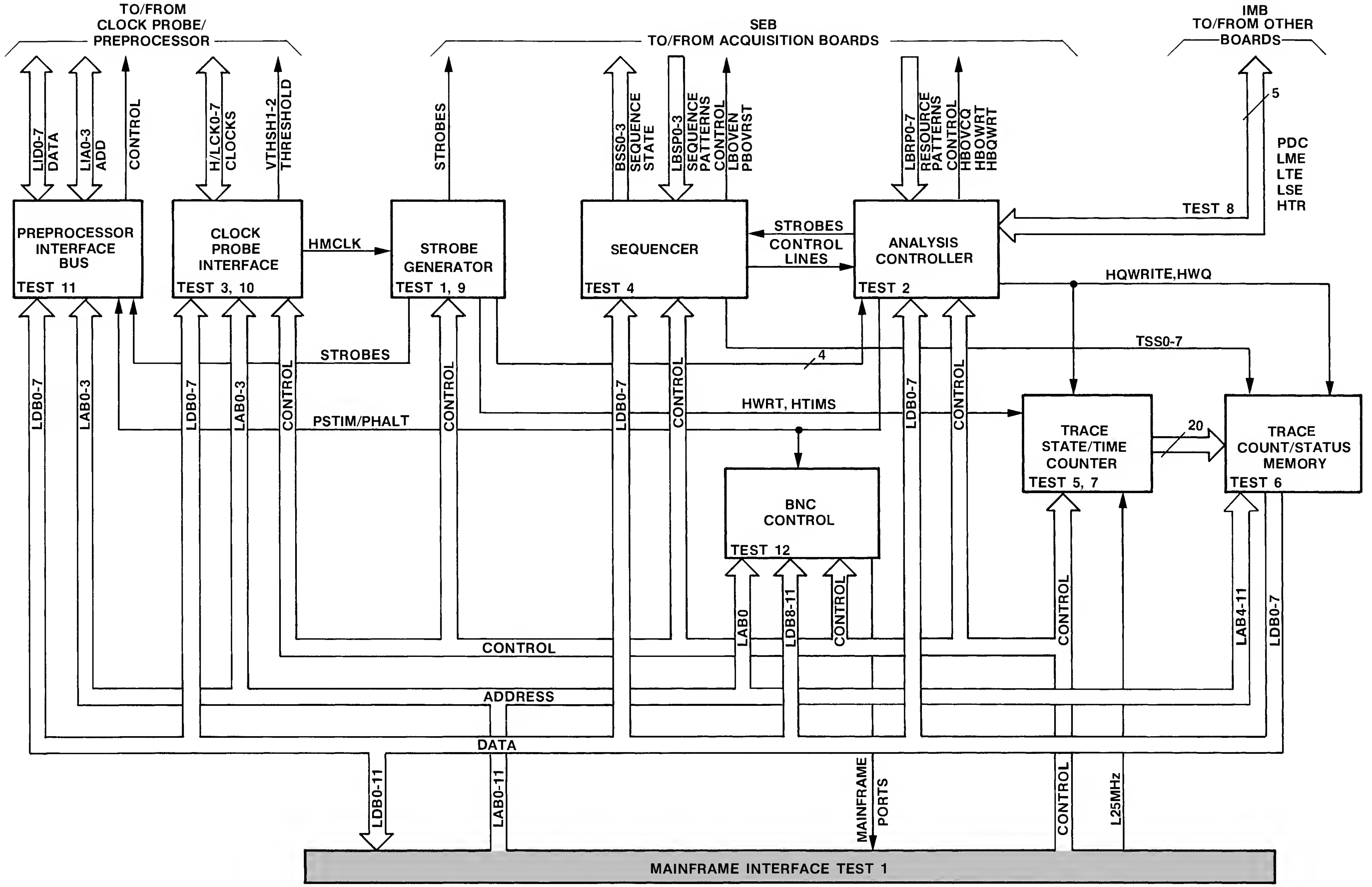
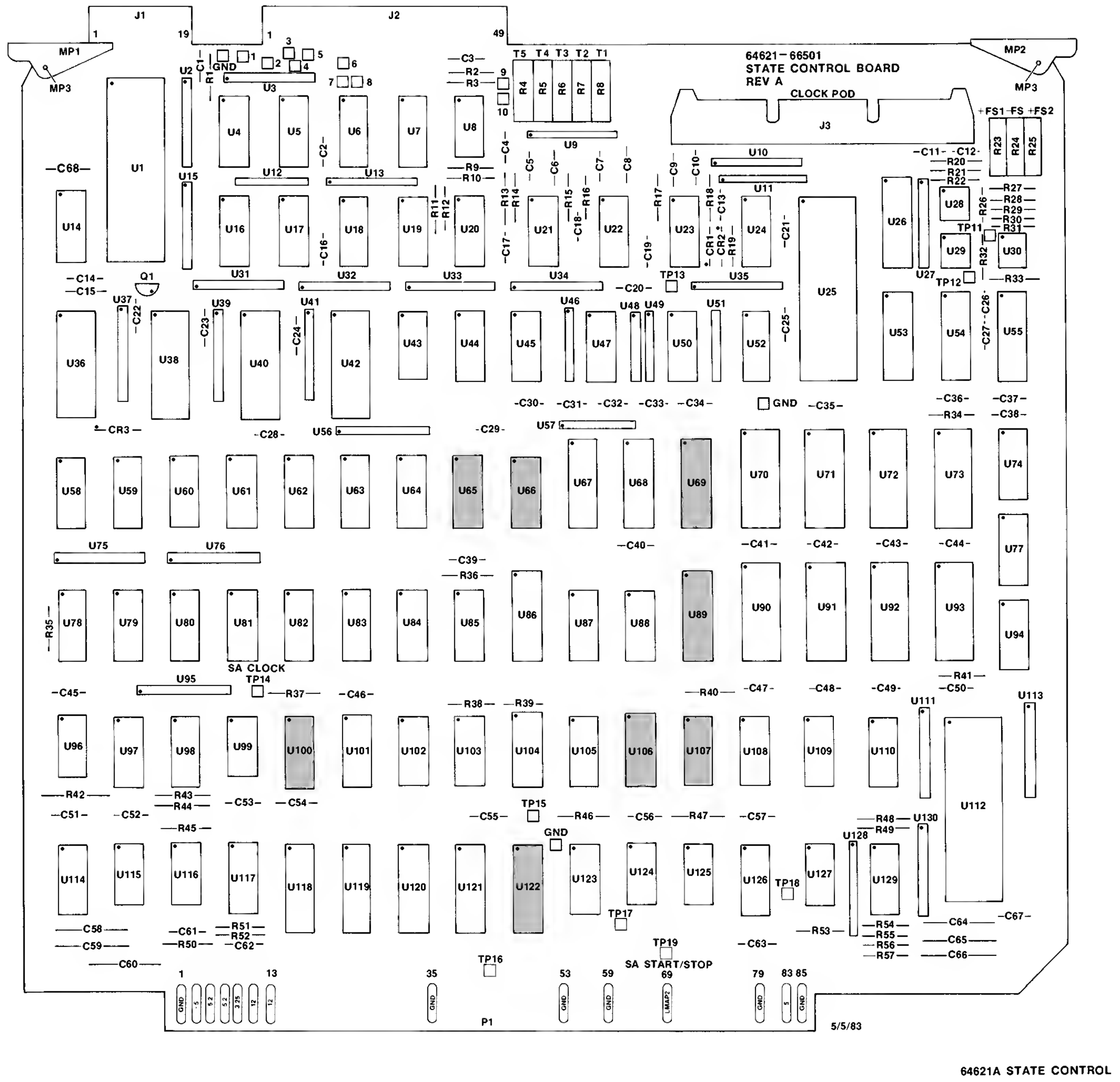


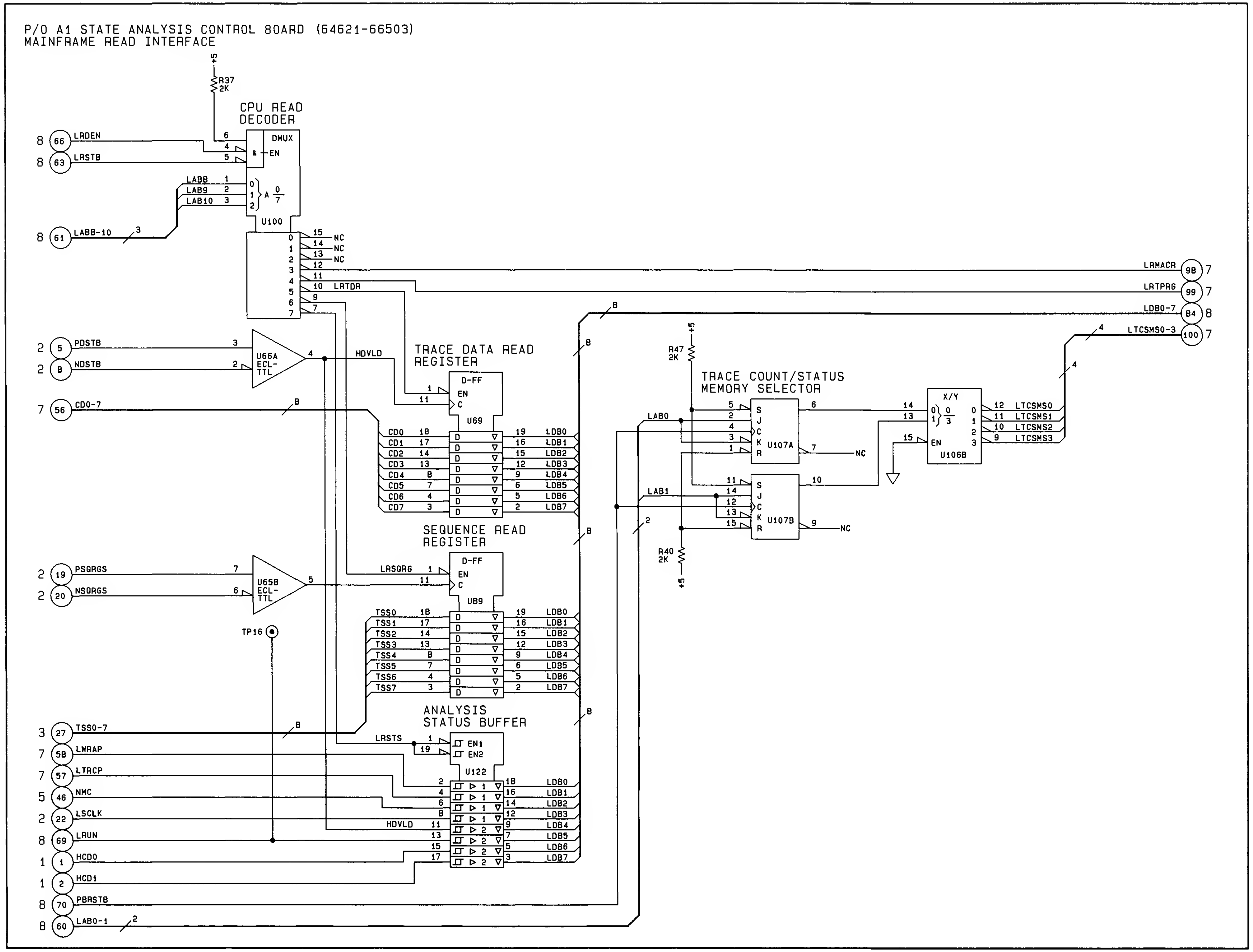
Figure 8-18.
Mainframe Write Interface



Block Diagram



Component Locator



9

ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U65,66	1820-1052	10125
U69,89	1820-1997	74LS374
U100	1820-1216	74LS138
U106	1820-1281	74LS139
U107	1820-1282	74LS109
U122	1820-2024	74LS244

PARTS ON THIS SCHEMATIC

R37,40,47
U65,66,69,89,100,106,107,122

POWER SUPPLY CONFIGURATION

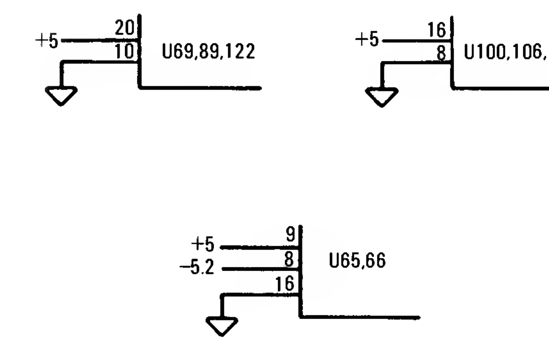


Figure 8-19.
Mainframe Read Interface

Product Line Sales/Support Key

Key Product Line
A Analytical
CM Components
C Computer Systems
E Electronic Instruments & Measurement Systems
M Medical Products
P Personal Computation Products
*** Sales only for specific product line**
**** Support only for specific product line**

IMPORTANT:These symbols designate general product line capability.They do not insure sales or support availability for all products within a line, at all locations.Contact your local sales office for information regarding locations where HP support is available for specific products.

HEADQUARTERS OFFICES

If there is no sales office listed for your area, contact one of these headquarters offices.

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Telex: 27835 hmea
Cable: HEWPACKSA Geneve

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Wanchai, **HONG KONG**
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